Design of Two-Stage Fully-Differential Operational Transconductance Amplifier Using a Standard 0.35µm CMOS Process

Tanya Vanessa F. Abaya[1], Frederick Ray I. Gomez[1, 2,*]

[1] Microelectronics and Microprocessors Laboratory, Electrical and Electronics Engineering Institute
College of Engineering, University of the Philippines, Diliman, Quezon City, Philippines 1101

[2] New Product Introduction Department, Back-End Manufacturing & Technology, STMicroelectronics, Inc.
9 Mountain Drive, Light Industry & Science Park II, Brgy. La Mesa, Calamba City, Laguna, Philippines 4027

[*]*Corresponding author's email: frederick-ray.gomez [AT] st.com*

ABSTRACT— ***The paper presents a design of a two-stage fully-differential operational transconductance amplifier (OTA) for a 10-bit 40-Msamples/s Nyquist rate analog-to-digital converter (ADC) using a standard 0.35µm complementary metal-oxide semiconductor (CMOS) process. A telescopic cascode topology is implemented as main stage, with common source amplifiers as output stage for the differential outputs. The open loop amplifier achieved a gain of 108dB, while the closed loop gain is at 12dB with settling time of less than 11ns for an accuracy of 0.5%. Total output noise achieved is 63.4uVrms. Loop unity gain bandwidth is 205MHz with phase margin of 77.6°. The design has a dynamic range of 88.3dB, and power consumption of 26.6mW from a 3V supply.***

Keywords---- OTA; CMOS; amplifier; ADC

1. INTRODUCTION

The Complementary Metal-Oxide Semiconductor (CMOS) Analog-to-Digital Converter (ADC), which is the target application of the designed Operational Transconductance Amplifier (OTA), is set to require a high open loop gain with settling accuracy of 0.5%. The OTA is also designed to dissipate minimum power and to have high dynamic range. Design considerations such as amplifier topology and device sizes, bias and values are discussed. Performance metrics and results are also presented. Conclusion and recommendations follow.

2. OTA TOPOLOGY

The first factor considered in choosing an amplifier topology is the required gain of the open loop amplifier. With the specifications set for functionality within the target ADC, the open loop gain is determined to be about 2400 as will be discussed in section II. This is in the order of $(g_m r_o)^2$ or $(g_m r_o)^3$. Topologies that will certainly satisfy this magnitude include a two stage amplifier with either telescopic or folded cascode first stage, a gain-boosted amplifier or a folded triple cascode. To avoid much complexity in the design process a two-stage topology is chosen.

Even though single-stage amplifiers such as the gain-boosted and triple cascode topologies only have two current legs passing thru significant current, dealing with pole-doublet is difficult especially in ensuring a fast enough settling. Also, single-stages produce less output swing (more so for a triple cascode). With an 86dB dynamic range requirement, the authors believe that despite the lower noise exhibited by the single-stage topologies, this would not be sufficient and output swing still needs to be maximized.

With two-stages on the other hand, additional dominant poles are introduced. These need compensation, which normally slows down the overall amplifier speed. However, overall two-stage amplifier design is fairly easy to design and optimize. The plan is to concentrate on the gain requirement in designing the first stage, while the second stage will be optimized for the needed output swing and for driving the capacitive load.

Implementation of the amplifier main stage has been chosen as a telescopic cascode topology over a folded cascode for the reasons that follow. While better power supply and common mode rejection is offered by the folded cascode, these parameters were not of topmost priority in this particular OTA. In terms of output swing, a telescopic cascode has lower output swing by only one V_{dsat}, and as stated earlier, output swing is not much of a concern in the first stage. Current consumption, parasitic capacitances and noise factor is also larger for the folded cascode, making it less attractive for this OTA.

The input transistors of the telescopic cascode stage are NMOS devices to maximize gm/Id. For the second/output stage, a common source amplifier for each differential output was utilized as typically done. Differential amplifiers as output stage would be more complicated due to the design of another common mode feedback circuit. In addition, the tail current transistor for the diff amp will only consume voltage headroom, thus lowering the output swing.

To ensure stability of the amplifiers, miller compensation is used despite the cascode compensation's better high frequency performance. Miller compensation however, can be easily designed and will introduce non-negligible noise depending on how the circuit is compensated.

The schematic design of the overall amplifier is illustrated in Figure 1.

To bias the nodes in the amplifier, a biasing network is needed and thus designed. The luxury of having an ideal current source (that would not cause mismatch) for the biasing allows for the use of a ratioed biasing. Figure 2 shows the biasing network.

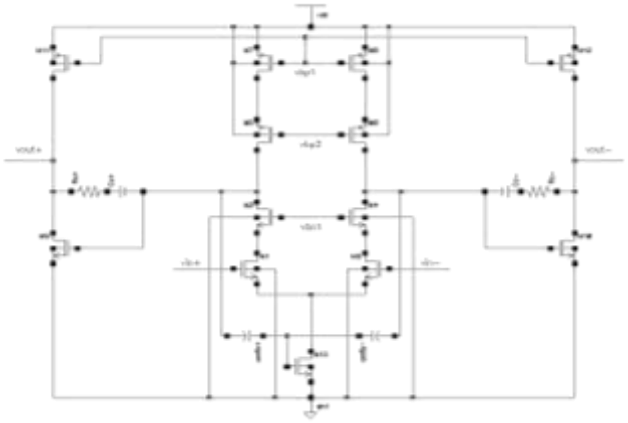

Figure 1. Two-stage fully-differential OTA.

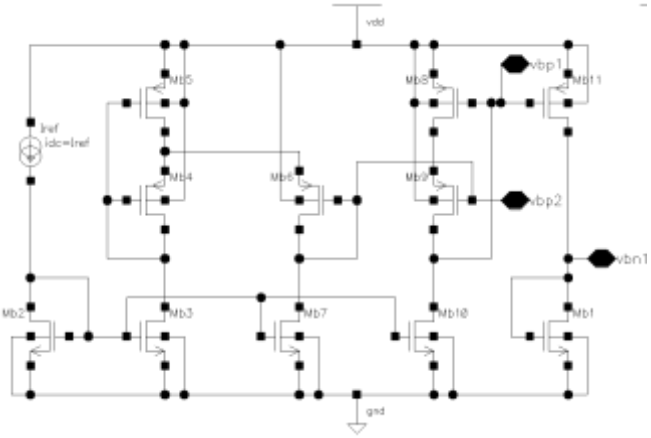

Figure 2. Biasing network for the OTA of Figure 1.

3. DESIGN PROCEDURE

A. Open Loop Gain and Static Error

The design of the open loop amplifier started with the determination of its gain. Both feedback factor *F* and static accuracy $\varepsilon = \varepsilon_s + \varepsilon_d$ dictates the gain via Eq. (1).

$$A_{vo} = \frac{1}{F\varepsilon_s} \qquad \text{Eq. (1)}$$

The feedback factor F is found from Eq. (2). The closed loop gain *c* is set at 4 and the input capacitance, which is about C_{gs1}, is chosen equal to the feedback capacitor. Thus, F=1/6.

$$F^{-1} = 1 + c + \frac{C_{in}}{C_f} \qquad \text{Eq. (2)}$$

The static error is assumed to be half of the total settling accuracy, which is in this case 0.005. The ε_s is then 0.0025. From here, the open loop gain is determined to be at least 2400.

B. Dynamic Range

The dynamic range (DR), which is a measure of the signal to noise ratio and mathematically defined in Eq. (3), requires high output swing and low noise. The output differential voltage Vod is set by the common source output stage. The maximum Vod possible is found from Eq. (4), which is essentially the voltage rail minus the minimum voltage drops across the two FETs. For the 0.35µm CMOS process, the minimum V* for strong inversion is found to be 150 mV. This is used for the NMOS devices. However, V* for the PMOS is set at about 250mV due to its lower transconductance. Maximum signal power is then 10log(3.25125)dB.

$$DR = \frac{P_{signal}}{P_{noise}} \qquad \text{Eq. (3)}$$

$$P_{signal} = \frac{1}{2}(V_{od})^2 = \frac{1}{2}(V_{dd} - V_9^* - V_{10}^*)^2 \qquad \text{Eq. (4)}$$

The noise power may be determined by Eq. (4). Noise is found to be $10\log(90.37\mu)^2$dB. Neglecting the noise from the cascode devices, this noise power is equal to the expression shown in Eq. (5), where α=1 and γ=2/3. Here, the effective load capacitance may be computed and is actually found to be about 4.8pF.

$$P_{noise} = \frac{2kT\gamma\alpha}{C_{Leff}F}\left(1+\frac{gm_7}{gm_1}\right) = \frac{2kT\gamma\alpha}{C_{Leff}F}\left(1+\frac{V_1^*}{V_7^*}\right) \qquad \text{Eq. (5)}$$

C. Settling Time and Unity Gain Bandwidth

Settling time and unity gain bandwidth (UGBW) is related by stability and compensation. If 40 % of the settling time is allotted for slewing and the rest for linear settling, a rough approximation of UGBW may be determined from Eq. (6) as 867MHz.

$$f_u = \frac{-\ln(\varepsilon_s)}{2\pi t_{lin}F} \qquad \text{Eq. (6)}$$

D. Bias Currents

The tail current passing through transistor M13 may be found from the results of the previous subsection and Eq. (7). With V_{o_step} as the maximum output swing determined earlier and slew rate SR equal to Iss/C_{Leff}, the tail current Iss is found to have a value 1.855mA.

$$T_{slew} = \frac{V_{o\_step}F - V_1^*}{SR(F)} \qquad \text{Eq. (7)}$$

For the output stage leg, the non-dominant pole is now considered. Assuming that this pole is at 3 times the UGBW, the current through the output stage may be determined using Eq. (8). As mentioned earlier, NMOS M9 should have a V* of 150mV for maximum swing while operating at strong inversion. The computed current is about 5.9mA.

$$p_2 = 3\times UGBW_{rad/s} = \frac{g_{m9}}{C_{out}} \approx \frac{2I_D}{V_9^* C_{Leff}} \qquad \text{Eq. (8)}$$

E. Device Setting

The lengths of the devices were determined first with some general considerations in mind. The PMOS current source transistors should be able to have a large overdrive voltage to minimize the noise factor and effective load capacitance and maximize the feedback factor. V* of M7 and M8 are set at 800mV. The lengths of this PMOS sources were set to 2µm. The remaining PMOS transistors M11 and M12 at the output node also have lengths of 2µm to increase the intrinsic output resistance and thus the gain of the amplifier. M5 and M6 are also sized in the same way.

M3 and M4 are optimized with M5 and M6. These four transistors need low V* but must push the second pole farther from the UGBW. Lengths for M3 and M4 are set at 1µm.

The input differential pair M1 and M2 should be set at minimum length (e.g. 0.35µm) for minimum overdrive voltage and relatively large gm/Id. However a length of 0.5µm is chosen taking into account the tradeoff between gain and parasitic capacitances that may degrade F.

All V* for these transistors is set also at 150mV.

The NMOS output pairs on the other hand, were sized having L = 1µm. This would be sufficient for a low V* of 150mV and still provide enough gain and low C_{Leff}.

For the tail transistor M13, it is designed with 0.5µm length for small V* to be able to help produce a maximum output swing. Notice that minimum length is not used as it is sensitive to process variations.

After the lengths have been set, plots of V* vs. Id were done with varying lengths, both for PMOS and NMOS. The plots shall be used to determine the widths of the devices given the current determined in a previous subsection.

Important device W/Id ratios for V*=150mV for the NMOS devices are

$$\frac{W}{I_D} = \frac{10\mu m}{45\mu A} \quad for \quad L = 0.5\mu m \qquad \text{Eq. (9)}$$

$$\frac{W}{I_D} = \frac{10\mu m}{40\mu A} \quad for \quad L = 1\mu m \qquad \text{Eq. (10)}$$

For PMOS devices, the ratios were taken using three V* values, all with a length of 2µm.

$$\frac{W}{I_D} = \frac{10\mu m}{3.8\mu A} \quad for \quad V^* = 150mV \qquad \text{Eq. (11)}$$

$$\frac{W}{I_D} = \frac{10\mu m}{8.63\mu A} \quad for \quad V^* = 250mV \qquad \text{Eq. (12)}$$

$$\frac{W}{I_D} = \frac{10\mu m}{64\mu A} \quad for \quad V^* = 800mV \qquad \text{Eq. (13)}$$

As an example, the computation for the PMOS current source transistors M7 and M8 is shown with Iss = 1.855mA. Thus, $Id_{7,8}$=927.5µA and $W_{7,8}$ = (10µ/64µ)(927.5µ) = 144.9µm.

F. Common Mode Feeback (CMFB)

The common mode feedback circuit utilizes a simple capacitive divider. The values for the capacitors may be determined with the use of Eq. (14). This equation is derived from stability considerations. For stability, the common mode UGBW is set at half its loop bandwidth.

$$F = \frac{2C_{CMFB}}{2C_{CMFB} + C_{gs13}} \qquad \text{Eq. (14)}$$

The value of the gate-source capacitance of M13 is easily found once the transistor dimensions have been set. This has been done as illustrated in the preceding subsection. The computed CMFB capacitance is 75.6fF, but this is only the minimum. To preserve the quality of the CMFB loop gain, C_{CMFB} should not be much smaller than C_{gs13}, which in this case is 756fF. C_{CMFB} is then decided to assume the value 500fF.

G. Closed-loop Capacitances

The feedback capacitance C_f is first determined. This is set equal to the gate-source capacitance of the input transistor M1 or M2. Therefore, $C_f = C_{gs1}$ = 378fF. Consequently, $C_s = C_r = 4C_f$ = 1.51pF. The load capacitance C_L is set at 200fF.

The tradeoff between settling time, noise and capacitance values were noted at this point in preparation of the possible tweaking of the capacitances during simulation.

H. Bias Network

The bias network should be able to output the following three voltage values: V_{bp1} = 1.33V, V_{bp1} = 1.27V, and V_{bp1} = 1.73V.

Device sizing is similar to that outlined earlier. The final schematic design is actually lifted from the work in [1].

4. FINAL DEVICE VALUES AND SIZES

Transistor sizes of the amplifier are presented in Table I together with the transconductance g_m, drain current I_d and g_m/I_d. Transistors for the bias network are detailed in Table II. Closed loop and compensation devices are listed in Table III with device values.

TABLE I. AMPLIFIER TRANSISTOR SIZES AND PROPERTIES

Device	W (µm)	L (µm)	gm (mS)	Id (mA)	gm/Id (V^{-1})
M1	500	0.5	16.13	1.045	15.43
M2	500	0.5	16.12	1.045	15.42
M3	400	1	11.65	1.045	11.15
M4	400	1	11.55	1.045	11.05
M5	700	2	5.846	1.045	5.596
M6	700	2	5.865	1.045	5.610
M7	144.5	2	1.587	1.045	1.519
M8	144.5	2	1.589	1.045	1.520
M9	200	1	7.274	7.135	1.019
M10	200	1	18.94	7.086	2.673
M11	780	2	15.16	7.136	2.125
M12	780	2	15.01	7.086	2.119
M13	802	0.5	30.67	2.09	14.67

TABLE II. BIASING CIRCUIT - TRANSISTOR SIZES AND PROPERTIES

Device	W (µm)	L (µm)
Mb1	1.8	1
Mb2	72	0.5
Mb3	72	0.5
Mb4	36	2
Mb5	15	0.75
Mb6	45	0.75
Mb7	72	0.5
Mb8	36	2
Mb9	45	0.75
Mb10	72	0.5
Mb11	18	2
Iref	250 µ A	

TABLE III. PASSIVE DEVICE VALUES

Device	Value
C_{CMFB}	500fF
C_c	1pF
R_c	200Ω
C_F	400fF
C_S	1.6pF
C_r	1.6pF
C_L	200fF

5. PERFORMANCE

The open loop and closed loop OTA is simulated and tested for the typical process corner. A summary of its performance is summarized in Table IV.

TABLE IV. AMPLIFIER PERFORMANCE SUMMARY

Device	Target	Achieved
Total output noise	$90uV_{rms}$	$63.4uV_{rms}$
Max differential output swing (above 2400 open loop gain)	2.6V	2.363V
Dynamic Range	86dB	88.3dB
Power Dissipation	minimum	26.6mW
Settling Time @ Max swing	11ns	8.55ns
Accuracy @ 11 ns	0.005	0.0027
Closed Loop Gain	4	3.96
Open Loop Gain	2.4K	247.5K
Loop Unity Gain Bandwidth	---	205MHz
Phase Margin @Vod=0	---	77.6°
Gain Margin @Vod=0	---	-21.36dB

6. SIMULATION RESULTS

I. Open Loop Gain

The gain of the open loop amplifier reaches a maximum of 245.7K as seen in Figure 3, which is a zoomed-in plot of the open loop gain vs. differential input Vid. The DC transfer characteristic is plotted in Figure 4. Clearly, the differential output voltage abruptly falls with a very small decrease in differential input voltage. Open loop AC response is shown in Figure 5 and 6. Large signal gain is also plotted, shown in Figure 7.

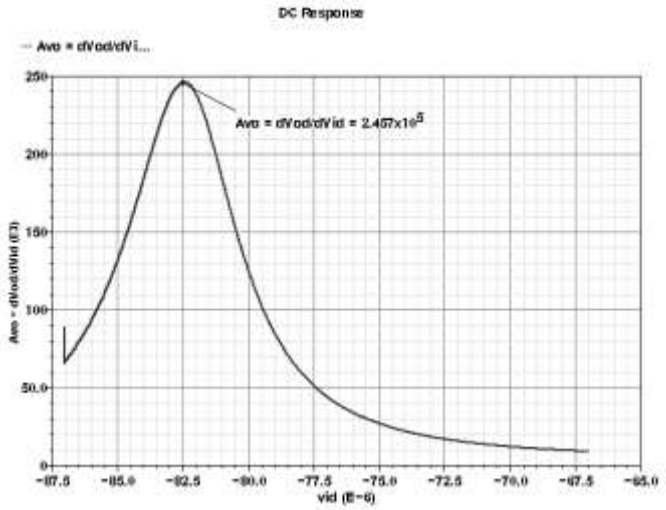

Figure 3. Maximum amplifier open loop gain.

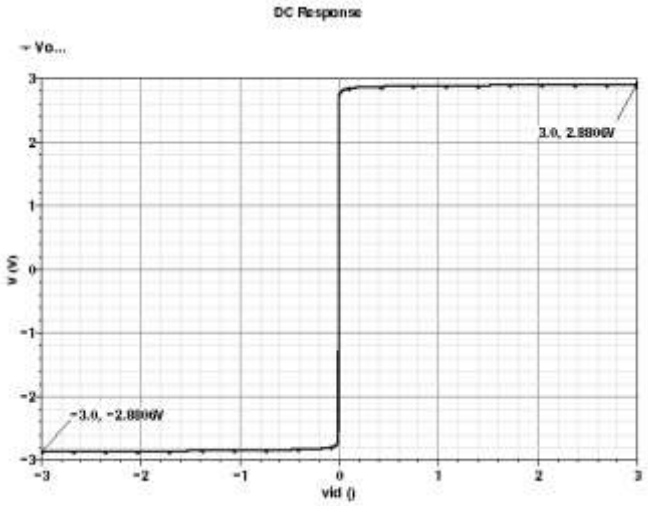

Figure 4. DC transfer curve of open loop amplifier.

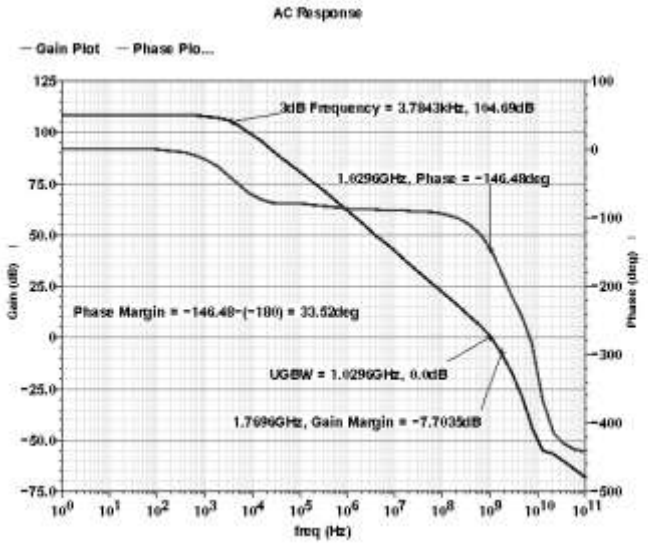

Figure 5. Open loop AC response for Vod = 0.

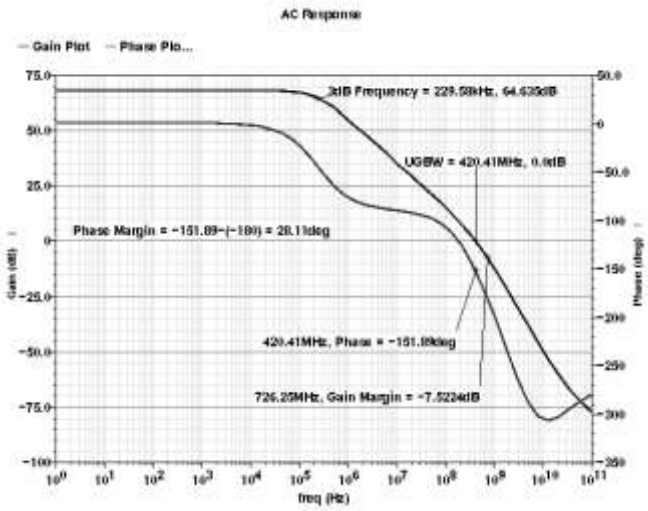

Figure 6. Open loop AC response for Vod = Vod_max.

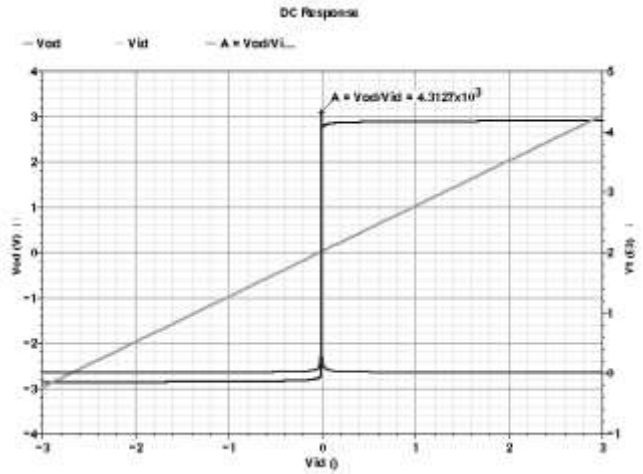

Figure 7. Large signal gain.

J. Stability

The Bode plot for Vod = 0 and Vod = Vod_max is shown in Figure 8 and 9. Phase and gain margins are clearly marked.

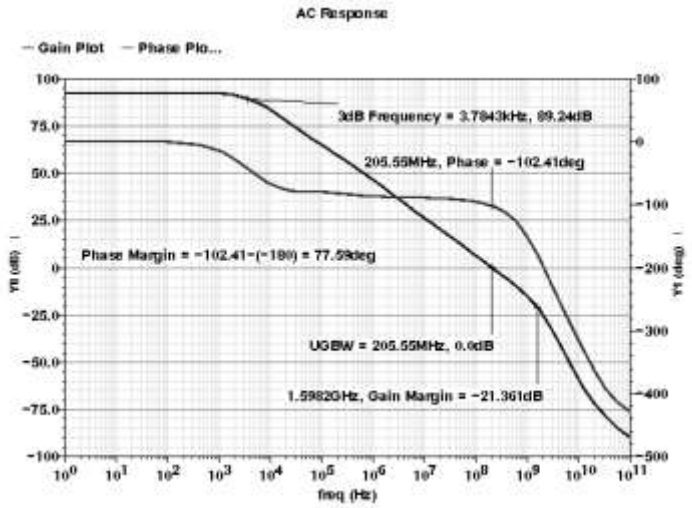

Figure 8. AC loop response for Vod = 0.

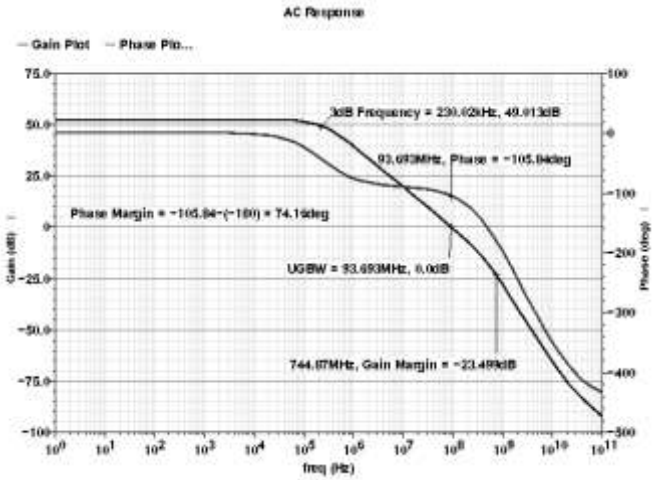

Figure 9. AC loop response for Vod = Vod_max.

K. Settling

In Figure 10, the settling time for an accuracy of 0.005 is shown with the markers. The table lists the values marked in this plot. Signal range downwards to meet settling requirements.

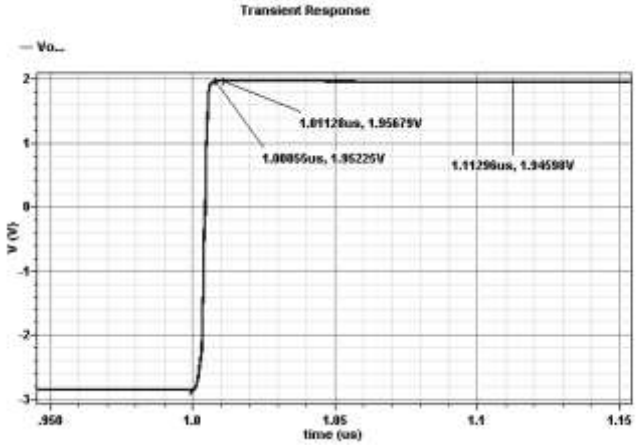

Figure 10. Settling time.

L. Power Dissipation

Figure 11 provides information on the power dissipation of the amplifier.

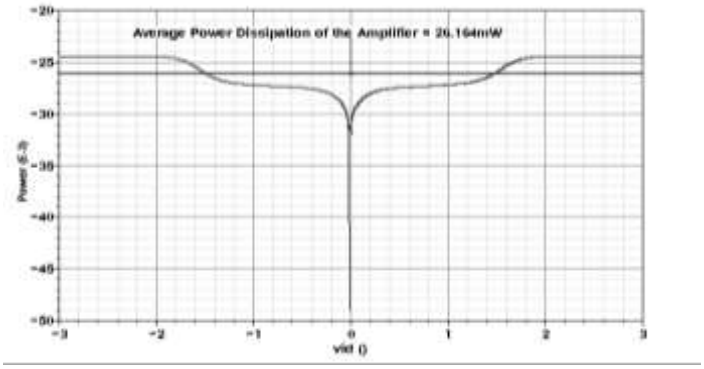

Figure 11. Power dissipation.

M. Noise

The plot of the noise determines the dynamic range of the OTA. Figure 12 and 13 shows output noise (in V^2/Hz) for Vod=0 and Vod=Vod_max, respectively. The total output noise power is determined by integrating output noise from 1Hz to 1THz. Results yield the same total output noise.

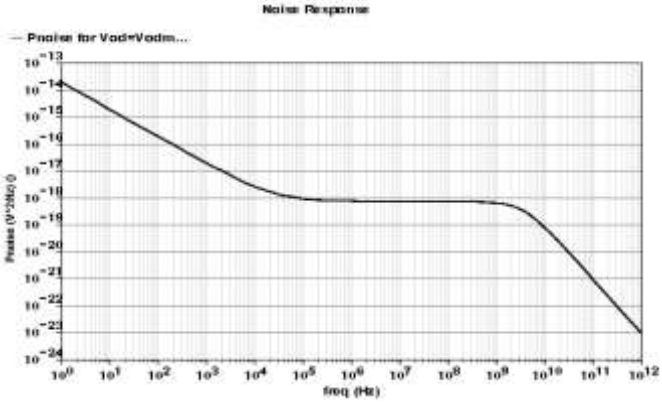

Figure 12. Output noise for Vod = 0 (V^2/Hz).

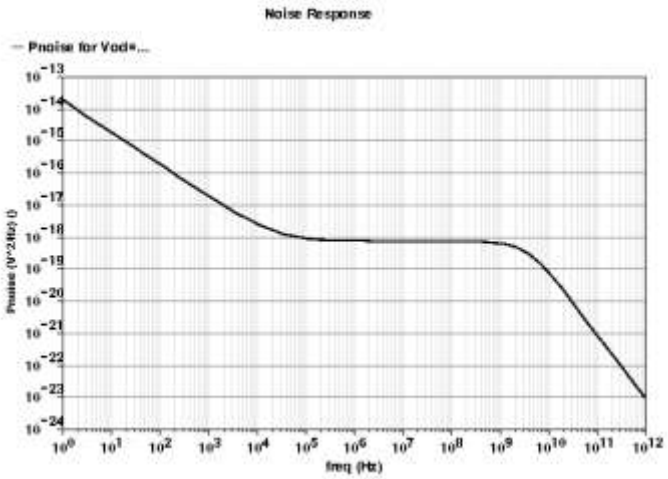

Figure 13. Output noise for Vod = Vod_max (V^2/Hz).

7. CONCLUSIONS AND RECOMMENDATIONS

The OTA designed met all specifications set by the CMOS ADC requirements. Design was started off with hand analysis followed by verification through simulations using Cadence software [2], which also includes a redesign stage for fine tuning and correction.

However, the target specifications were only tested for the typical process. Fast and slow process corners are recommended for study and comparison with hand analysis. Other parameters such as power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) should also be considered in this design.

Seeing that power consumption in this design is relatively large, techniques on lowering this power consumption is recommended to be employed. It is also a recommended to explore the single-stage differential operational transconductance amplifier.

8. ACKNOWLEDGMENTS

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