A Methodical Approach in Critical Processes Optimization of New Scalable Package Semiconductor Device for ESD Applications

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ABSTRACT— ***The technical paper presents a systematic approach to deal with a new product trend that will survive during assembly production ramp-up. The project was intended to determine the required process flow and platforms for high-density and high-complexity scalable device. Critical processes were shown and top reject contributor was addressed through methodological way by using statistical tools and in depth engineering analysis.***

The New Scalable Device is one of the newest and latest developed device in the plant, with main application as an Electrostatic Device (ESD) protection device. The device is considered high density as its 6" single wafer is equivalent to 400,000 units compared to conventional device consisting of only 1,000 units. Moreover, it is considered as a device with high complexity as state-of-the-art platforms were needed to satisfy its output process. The device has a very thin die and with the smallest total package dimension. The process of assembly manufacturing includes a step cutting method of wafers, compression molding, and in-strip testing, which are unlikely to be found on other semiconductor industries. Compared to the conventional and universal approach, complex errors and top reject contributor of identified critical processes were corrected and required process capability index was ultimately achieved.

Keywords— Scalable device; semiconductor package; IC; design of experiments; ESD

1. INTRODUCTION

In order to cope with the fast-paced technology in semiconductor industry, one should have a very good impression from the customer be it internal or external. This is one of the biggest challenges for any semiconductor company in order to maintain its competitive market position and value. "Satisfaction" is the right word and key factor in building good relationship with the customer. On the other hand, failure to provide customer expectation in terms of on-time delivery will result to possible business failure. This critical scenario should be avoided that's why a risk production or line stressing is being done in preparation to full production mode. A total of 10 to 30 lots are line stressed to capture all hindrances in the production line and thus corrected immediately to prevent delivery issues.

Misdeliveries or delinquency in view of customer was the scenario encountered during the line stressing and ramp-up of New Scalable Device (hereinafter referred to as Device A). With the continuing technology trends and state-of-the-art platforms [1] [2] [3], this technical paper will discuss how the burden was turned into milestones when top yield detractors of critical processes were addressed by in depth engineering analysis and utilizing statistical tools at early stage of production.

1.1 The Device on Focus

Device A is a diode with a single wire connection, with main function as an ESD protection device for mobile phones and computer applications. Shown in Figure 1 is the package illustration, top view and cross-section view of Device A.

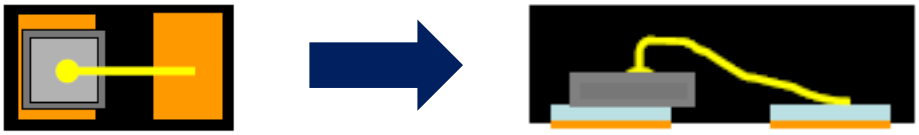


Figure 1: Device A package construction

Device A is compared in Figure 2 to the size of a grain, to illustrate the complexity of the process and the device itself with primary consideration on the total package dimension. As the size becomes smaller, process and device complexity become more challenging. Device A is considered high density as its 6" single wafer is equivalent to 400,000 units

compared to conventional device consisting of only 1,000 units. In addition, it is considered as a device with high complexity as state-of-the-art platforms were needed to satisfy its output process.

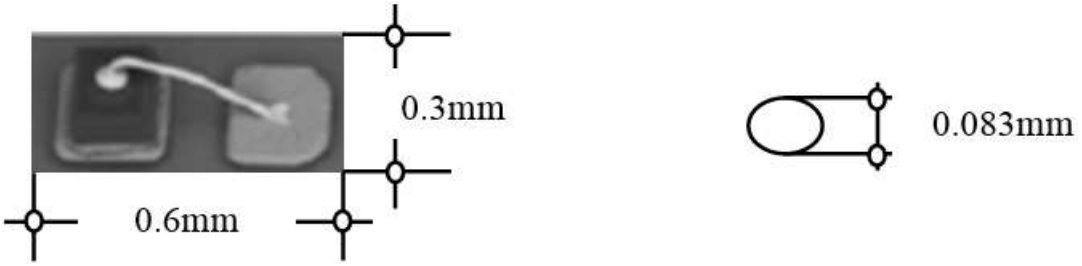


Figure 2: Comparison of Device A to size of a grain

1.2 Full Process Flow

Complete process flow for Device A starting from Pre-Assembly to Back-end Assembly until Test and Finish and Packing is shown in Figure 3.

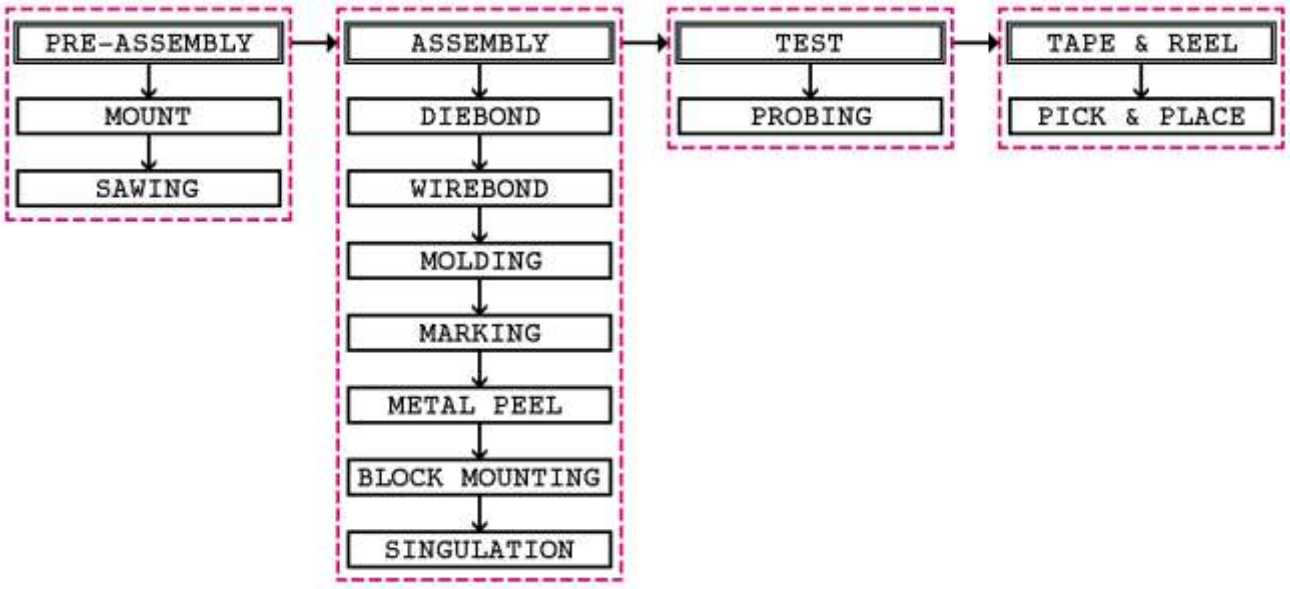


Figure 3: Device A complete process flow

Three critical processes were identified using risk analysis, as identified in Table 1. Evaluation was made before the risk build to accelerate confidence on line stressing. Furthermore, Potential Risk Analysis was given contingency plans and created corrective actions.

Table 1: Potential risk analysis of Device A

Item	Identified Risk	Resulting Potential Risk	Evaluation Before Action			Identified Action
			Probability	Impact	Class	
1	Wafer sawing quality (conductive die-attach film adhesion, small dice dimensions, chippings, excessive dice-off	▪Low yield ▪Reliability	9	9	A	Sawing process using step-cut method, wafer staging
2	0.3mm package molding, package molding defects, voids, incomplete fill	▪Low yield ▪Reliability	9	9	A	Capability using compression molding technology
3	Marking misalignment due to small mark area	▪Low yield ▪Reliability	9	9	A	Marking alignment optimization, precision alignment jig
4	Tape and reel, flip chip packing	▪Low yield ▪Reliability	9	9	A	Capability using flip-chip technology
5	In-strip test over rejections (singulated units)	▪Low yield ▪Reliability	9	9	A	Implementation of reverse process flow

Reject contributors on the identified critical processes are shown in Figure 4. Wafer Saw, Mold and In-Strip Test or Final Test experienced deviations or output abnormalities as a result of not optimized parameters which are normally attributed to newly introduced device.

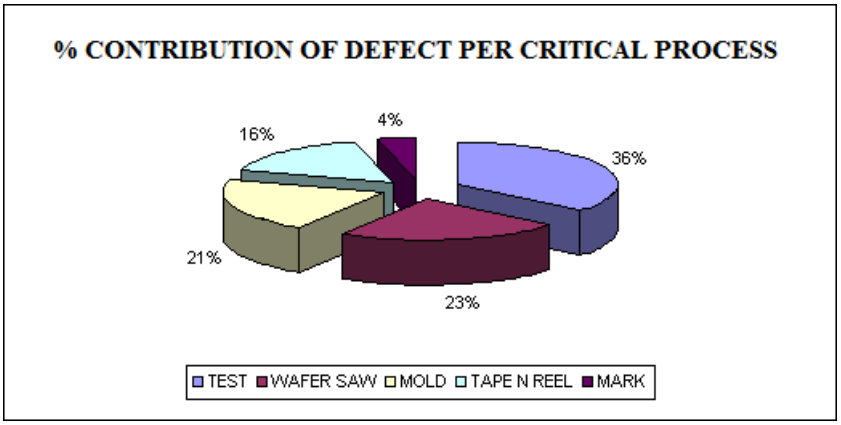


Figure 4: Defect per process contribution

1.3 Process Pareto Diagram of Rejects per Critical Process

Wafer Saw process contributed to the 23% defects as illustrated in the graph of Figure 4. And of these 23% defects, Pareto diagram on Figure 5 shows die chipping was the top contributor, followed by dice off and broken wafer. Other critical processes affecting the line stressing mode that have significant contribution of defect are the Final Test and the Mold encapsulation processes with 36% and 21% contribution, respectively. Parameter optimization is one of the factors to be checked as this type of device is to be built for the first time in the plant. Benchmarking for similar device to other sites is being considered to have a baselining on critical process parameters. Figures 5 also presents the Pareto diagram of reject contribution for the Final Test and Mold processes, respectively, with actual Defect Parts Per Million (DPPM) intentionally not given.

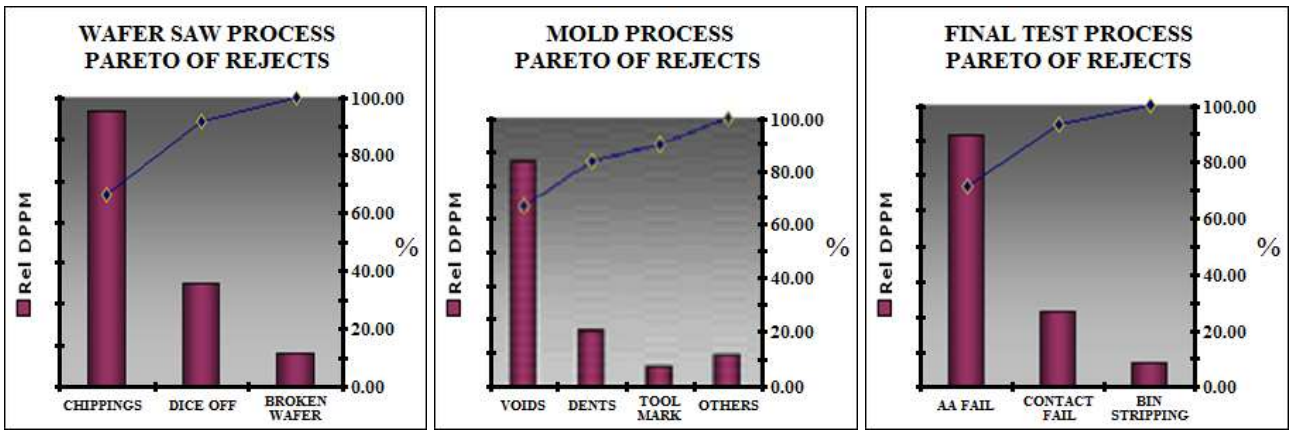
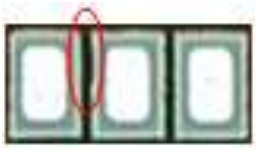
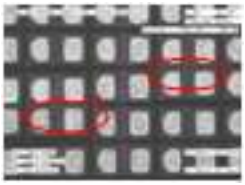


Figure 5: Pareto diagram of rejects showing the top contributor (actual DPPM values intentionally not shown)

1.4 Problem Statement

Top rejects based on Pareto diagram of identified three critical processes substantially affect the yield and delivery during production stressing performance. With this, optimization is highly recommended before it reaches the full production release. Table 2 summarizes the top defect signatures of the critical processes. Further analyses and investigations of failures are made by collecting actual reject samples from critical processes. This will serve as lead in the investigations and formulation of corrective actions.

Table 2: Top defect signature of critical processes

Critical Process	Top Defect Signature	Criteria	Remarks
Wafer Saw	 Chippings	Not allowed to reach active metallization	Failed
Mold	 Voids	Not allowed	Failed
Final Test	 Auto Align (AA) Fails	Not allowed	Failed

2. LITERATURE REVIEW

Three critical processes of Device A earlier identified are the Wafer Saw, Mold, and Final Test processes. Details of each critical process and their corresponding top reject contributor are further discussed in this chapter.

2.1 Wafer Saw (Critical Process # 1)

Device A is considered as Low-K (a material with a small dielectric constant) wafer (very thin), thus sawing becomes a critical process. When abrasive blades cut or groove the material, they are actually grinding and removing it. The mechanism is similar to that of a metal saw: the gaps between the teeth of the saw whisk material away from the point of processing. These gaps, called chip pockets, are encircled in Figure 6.

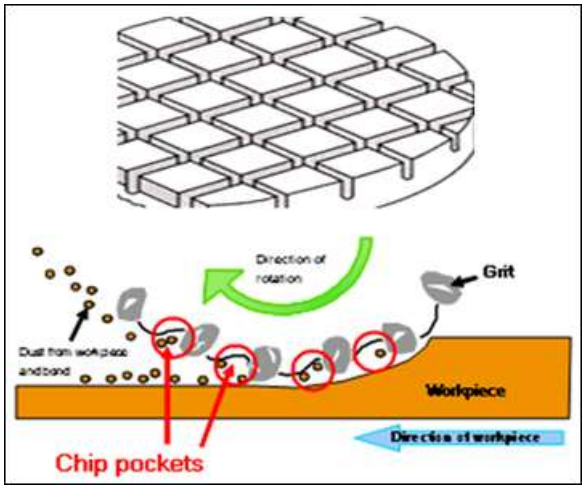


Figure 6: Wafer saw mechanism showing how chipping pockets occur

New blade has diamonds covered wholly by the bonding material and no diamonds (hammers) are exposed on the surface [4]. Therefore, diamonds cannot make cracks. If you cut the wafer with this condition, big chippings may happen, or the blade may be broken depending on the cutting speed [5]. After dressing, bonding material is removed and diamond comes out on the surface as shown in Figure 7. At the same time, small hole called chip pocket is created. This chip pocket will bring cooling water in the cutting area and will draw out small cutting chips temporarily storing in this pocket.

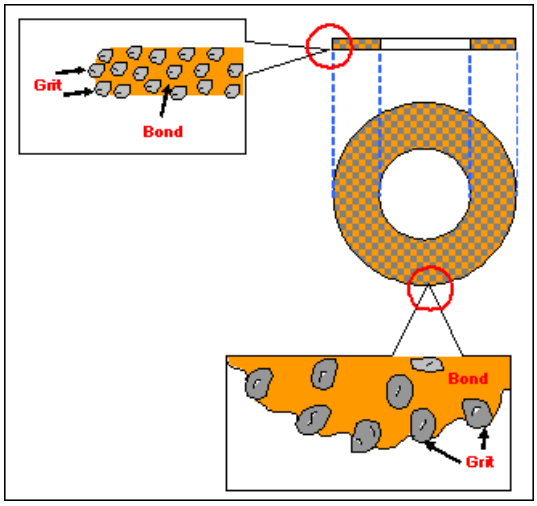


Figure 7: Elements of blade structure and their purpose

The blade is composed primarily of grit and bond. The grit is what actually performs the processing. The bond's role is to the hold the grit in place. Chippings are generally present on a new blade. Hence, blade dressing and precut are needed to be performed, as illustrated in Figure 8. Blades are dressed before shipment. However, precut operation is still needed to condition the blade and to true the outside diameter, removes excess binder material or loose diamond particles, and minimize the load, creating a cooler and freer cut resulting to minimize occurrence of chippings.

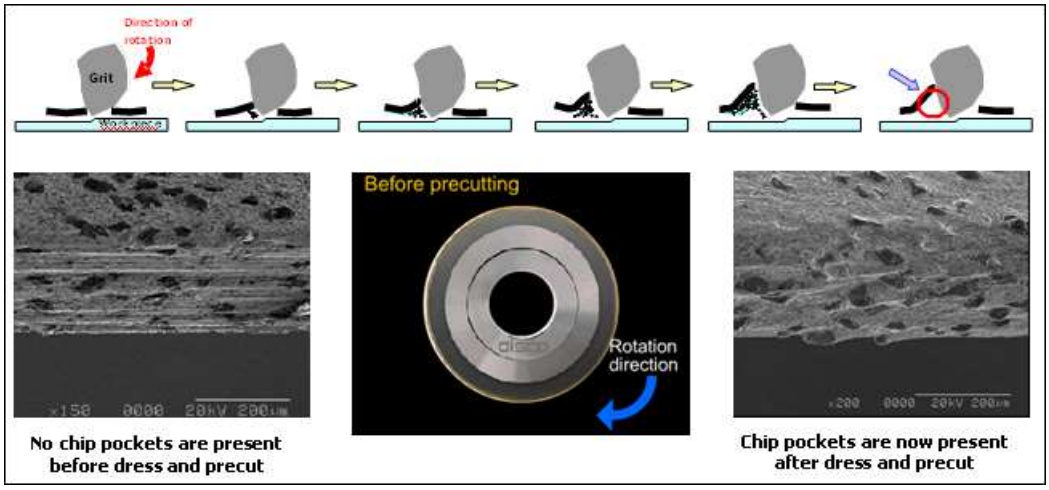


Figure 8: Dressing and precutting mode

Dressing and Pre-cutting cannot simply eradicate chippings when using a single blade. Single blade carries a greater process load and thus, results in an increase in surface chippings. That is why a Step-Cutting mode was introduced to minimize chippings during cutting. Step-Cutting method shown in Figure 9 is done using two blades (Z1 & Z2). The Z1 will partially cut the wafer and Z2 will totally cut the wafer making it stress relief.

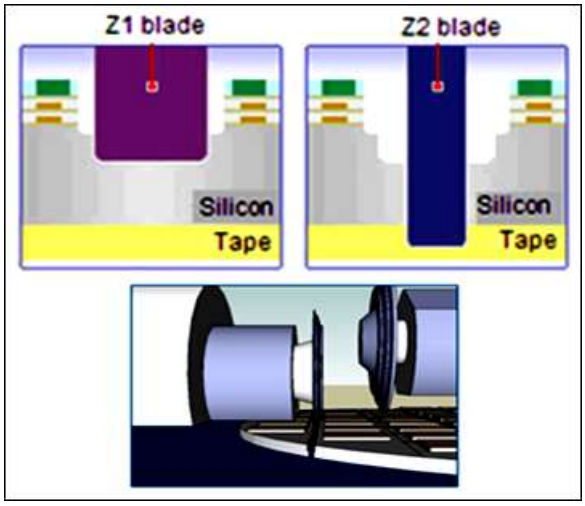


Figure 9: Step-cutting method

2.2 Compression Mold (Critical Process # 2)

One of the integral components in the production of semiconductor Integrated Circuits (IC) is the molding compound [6], a packaging material for encapsulation to protect the IC from external environment. Unlike conventional transfer molding, Device A process uses compression molding [7] with ultra-fine filler compound, shown in Figure 10.

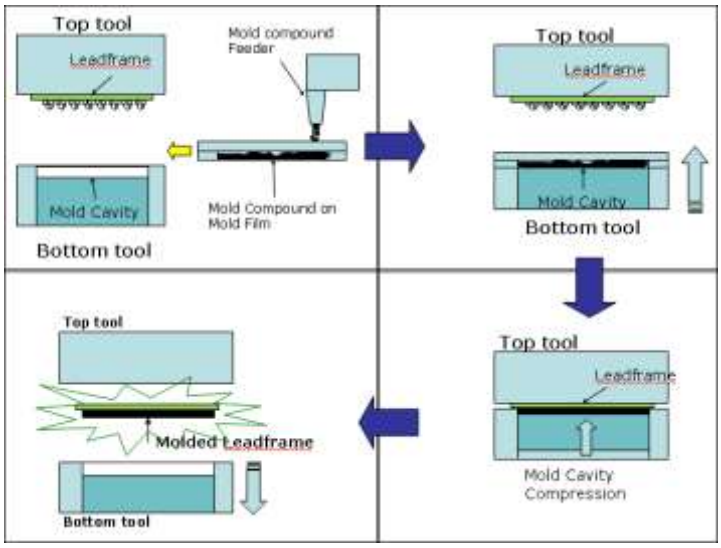


Figure 10: Compression molding mechanism

The advantages of compression molding system are zero/less wire damage, good filling on narrow gap on die, and no cull/no runner. The technology was necessary for Device A due to the requirement of narrow mold thickness. With this, device is prone to voids during molding, thus voids became the top reject contributor. Mold voids are commonly easy to correct, but this requires a thorough parameter optimization through design of experiments (hereinafter referred to as DOE). DOE was done to achieve desired parameter range for molding process taking into account the critical input and output responses. Moreover, mold voids is the critical and primary output response.

2.3 In-Strip Test (Critical Process # 3)

Conventionally, units are tested after singulation, but in limited quantity. In this era of technological advancements of high density device, In-Strip Testing was developed. The dilemma however is the contacting issues, as illustrated in Figure 11. Device A is consist of 12,740 singulated units making it prone to alignment failures compared to conventional device consisting of less than 500 units.

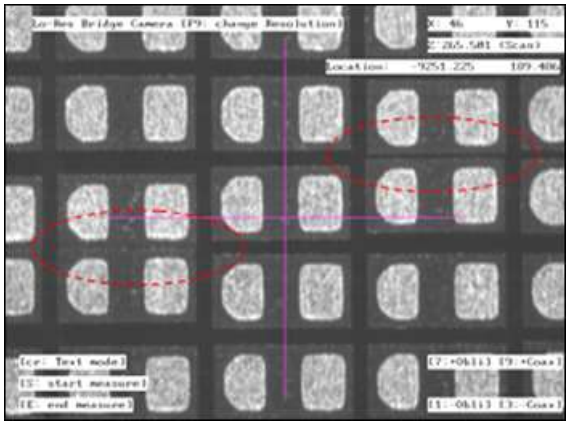


Figure 11: Singulated units showing narrow gaps in between units, resulting to auto align (AA) failures

3. METHODOLOGY

To mitigate the chippings, DOE was done on the three input variables at wafer saw, dressing, precutting, and step-cutting mode, as summarized in Table 3.

Table 3: DOE matrix for wafer saw process

Process	Run 1	Run 2	Run 3	Run 4	Run 5
Dressing	Yes	Yes	No	No	Yes
Precut	No	Yes	Yes	No	Yes
Step-cut	No	No	Yes	Yes	Yes

DOE for compression mold was conducted with the objective to determine and define window for critical parameter range, thus eliminate mold voids. Shown in Figure 12 is the DOE matrix prepared using SAS-JMP, a system software calculating automatically the combination of runs.

3x3 Factorial
Design 3x3 Factorial
Screening
Model

Columns (4/0)
Pattern
MOLD TEMP *
CURE TIME *
MOLD VOIDS *

	Pattern	MOLD TEMP	CURE TIME	MOLD VOIDS
1	11	170	160	.
2	22	175	180	.
3	12	170	180	.
4	13	170	200	.
5	23	175	200	.
6	32	180	180	.
7	21	175	160	.
8	33	180	200	.
9	31	180	160	.

Figure 12: 3x3 full factorial design for mold voids

Full factorial design with a total of nine runs was created. At SAS-JMP, mold temperature and cure time were identified as the most critical parameters that will cause mold voids defect. Results of each run will be discussed in the results section.

In order to eliminate alignment issues, reverse flow was employed. The reverse flow which is testing prior singulation will ultimately resolve Auto Align and other singulation related defects as testing will be done on a strip form. Table 4 shows the matrix to help identify and address the AA failure.

Table 4: 4M+1E matrix to identify and address AA failures, with significant factors denoted in *

Man	Machine	Method	Material	Environment
Prober operator	Prober	Strip loading *	Strip *	N/A
Singulation operator	Sawing machine	Strip sawing *	Blade	N/A
Strip mount operator	Strip mounter	Strip mounting *	Mounting tape Mounting jig *	N/A
		Sawing before testing *		N/A

4. RESULTS AND DISCUSSION

Optimum process parameters were attained based on the results of the DOE that addressed the top reject contributors to the critical processes. Comparative tests were used to statistically validate the results, with the aid of SAS-JMP, a statistical software which greatly facilitates in analyzing the data and relieves much of the tedious calculation. All-Pairs Tukey-Kramer test was preferably used to give a more conservative estimate of results as compared to the other tests.

4.1 Wafer Saw Optimization to Address Chippings

DOE results confirmed that when blade is Dressed, Precut and used Step-Cutting mode, it gives minimal surface chippings. Figure 13 shows the statistical results with All-Pairs Tukey-Kramer test revealing a highly significant difference on Run 5 in terms of surface chippings among other runs.

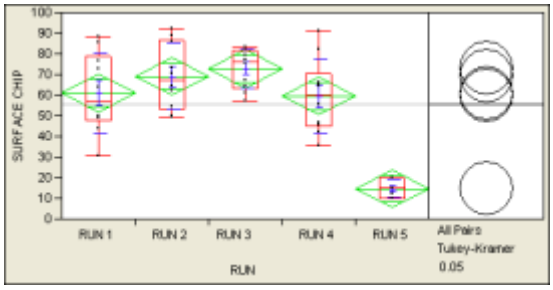


Figure 13: Statistical graph of analysis of variance implying significant difference on Run 5

4.2 Compression Mold Optimization to Address Voids

During development the initial problem encountered was package voids every shot. Together with the mold machine supplier [7] and the mold compound supplier, DOE was performed using a matrix of different batch of mold compound and sets mold parameter. The DOE result is illustrated in Figure 14.

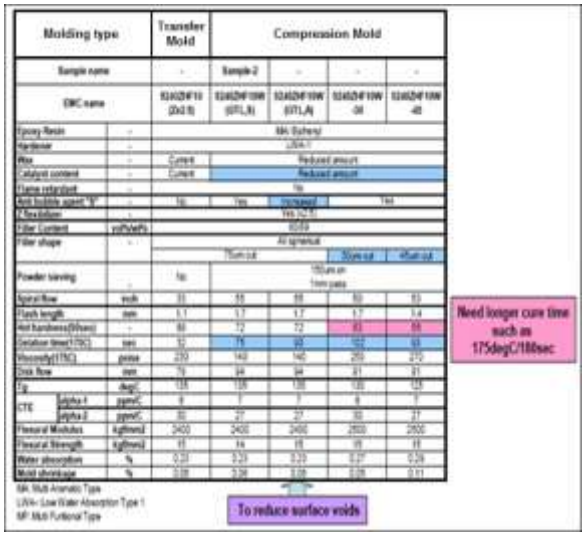


Figure 14: DOE Matrix to optimize voids during compression molding process

DOE results of compression molding showed that optimum parameters in terms of voids can be achieved by using the 175 degrees Celsius and 180 seconds curing time regardless of molding compound used.

4.3 In-Strip Test Optimization to Address AA Fails

Figure 15 presents the comparable yield and test results during preliminary evaluations when reverse flow is implemented without AA failures.

All yields prior singulation are higher compared to the yield after singulation.

	Wafer	Gross	Pass	Yield	Fail	Bin 1	Bin 5	Bin 7	Bin 14
un-singulated	1	12736	12720	99.87%	16	12720	0	0	16
	2	12736	12709	99.79%	27	12709	5	0	22
	3	12736	12725	99.91%	11	12725	1	0	10
	4	12736	12710	99.80%	26	12710	0	1	25
singulated	1	12736	12716	99.84%	20	12716	0	0	20
	2	12736	12703	99.74%	33	12703	6	0	27
	3	12736	12717	99.85%	19	12717	1	0	18
	4	12736	12570	98.70%	166	12570	4	1	161

Figure 15: Yield comparison of un-singulated vs. singulated units causing AA fails

Although preliminary evaluations were made, large scale validation is needed as reverse flow is considered major change and will undergo process change review. It will take a longer time to implement due to its major change requirements. AA fails was still further investigated while waiting for the reverse flow to be put in place. Cause and effect matrix was tabulated to identify other factors contributing to this defect.

After identifying the potential causes and validating its contribution on AA fails, the following solution and error proofing was created. Solution was put in place based on cost, applicability, effectiveness and impact to the problem. During the course of brainstorming, a breakthrough idea came out that will defeat all odds. AA fails will ultimately resolve by reversing its process, as AA fails occur when the products are singulated brought about by traditional way of testing units after singulation, this time testing was done on a strip form prior singulation thus eliminating the problem.

Table 5: Solution validation matrix

Potential Causes	Actions	Error Proofing Level	Status
Excessive vacuum force on prober chuck	Install air regulator / vacuum reducer near chuck area	2	Implemented
Insufficient edge stopper to prevent block from moving during mounting	Redesign mounting jig with edge stopper to prevent block from moving during mounting	2	Implemented
Too many air voids in between unit and tape upon mounting	Cleaning of block prior mounting	3	Implemented
Movement of singulated units causing AA failures	Implementation of reverse flow Implement testing prior singulation process	1	Implemented

4.4 Verification of Results

After the implementation of the identified solutions, level of rejections was monitored. Shown below in Figure 16 are the results before and after the solution implementation.

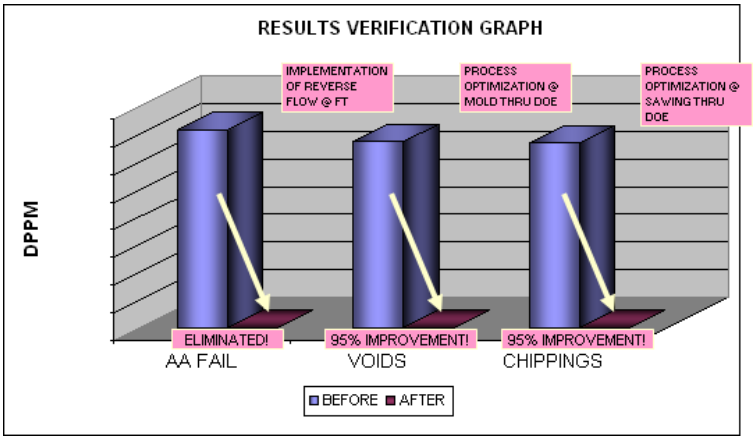


Figure 16: Improvement after implementation of the corrective actions (actual DPPM values intentionally not shown)

Significant reduction in the level of rejects were achieved and the three critical processes and their corresponding top reject contributor become stable after the implementation of corrective action. A Poka-Yoke approach by reverse flow lead to the elimination of AA Fails and a remarkable improvement of 95% gained after the implementation of corrective actions for voids and chippings through comprehensive DOE. This is a good indication of manufacturing preparedness for full production mode.

5. CONCLUSIONS AND RECOMMENDATIONS

Although, a flawless New Package Introduction cannot be realized immediately, process optimizations play a vital role to as early as line stressing stage, before full production release can be granted. Employing an in-depth engineering analysis and with the aid of statistical analysis in solving top reject contributors were presented on this technical paper. Using the knowledge and understanding on statistical tools led us to pinpoint the critical processes that need special attention and focus during risk production. Top reject contributors were identified using Pareto analysis and problems were addressed using DOE and solution validation was employed to formulate effective corrective actions. Chippings at wafer sawing can be addressed by doing dressing, precut and step-cutting mode. Voids induced during compression molding can be eliminated using optimum parameters via DOE of 175 degree Celsius and 180 seconds curing time. Auto align failure can be eliminated by thinking out-of-the-box idea like that of reversing its process.

It is recommended that the corrective actions identified, sustained, and monitored to maintain the rejects on the acceptable PPM level as some of the identified rejects cannot be zeroed out or eliminated. This technical paper showed how to dig and identify contributing factors on the top rejects of critical processes during early stage of production and employing in depth engineering and statistical analysis to attain significant improvements and recommends a permanent fix to production line. It is imperative that when new devices are coming in, critical processes are needed to be identified and that appropriate corrective actions and solutions be made so that when full production are set, deliveries will not be at stake.

As the application of Device A is for ESD protection, it is highly recommended, if not necessary, that the assembly manufacturing of Device A observe proper ESD controls. . Opportunities presented in [8] could be very useful to help ensure ESD check and controls. Ultimately, continuous improvement is important for sustaining the quality excellence of any product and of the assembly plant.

6. ACKNOWLEDGMENT

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7. REFERENCES

[1] Y. Liu, S. Irving, T. Luk, and D. Kinzer, “Trends of power electronic packaging and modeling”, 10th Electronics Packaging Technology Conference, Singapore, December 2008.
[2] Y. Tsukada, K. Kobayashi, and H. Nishimura, “Trend of semiconductor packaging, high density and low cost”, 4th International Symposium on Electronic Materials and Packaging, Taiwan, December 2002.
[3] A. Sumagpang Jr. and A. Rada, “A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms”, Presented at the 22nd ASEMEP Technical Symposium, Manila, Philippines, June 2012.
[4] DISCO Corporation, “Electroformed bond hub blades – high performance hub blades that take on the challenges of cutting”, https://www.disco.co.jp/eg/products/catalog/pdf/nbczh.pdf
[5] DISCO Corporation, “Fully automatic dicing saw – advanced performance for 300mm dicing”, https://www.disco.co.jp/eg/products/catalog/pdf/dfd6361.pdf
[6] H. Ardebili, J. Zhang, and M. Pecht, Encapsulation technologies for electronic applications, 2nd ed., William Andrew Applied Science Publishers, Elsevier, USA, October 2018.
[7] TOWA Corporation, Compression Molding System PMC 1040 Operational Manual, 1st ed., Kyoto, Japan, September 2008.
[8] F.R. Gomez and T. Mangaoang Jr., “Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-mr leadframe devices”, Journal of Electrical Engineering, David Publishing Co., vol. 6, no. 4, pp. 238-243, July 2018.