Design of a High Frequency and High Sensitive Low Noise Amplifier

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ABSTRACT— ***In most applications of the microwave amplifiers not only high amplification is desirable, but the usable bandwidth is also of importance. An ordinary amplifier can't operate at microwave ranges because of their inherent parasitic parameters and thus, it is necessary to design a microwave amplifier, which is free from above bottlenecks. This work presents the design and simulation of a High frequency low noise amplifier (LNA). with high gain, high sensitivity and low noise using Bipolar Junction transistor (BJT).. The design methodology requires analysis of the transistor for stability, proper matching, network selection and fabrication. The BFR 193 BJT Transistor was chosen for the design of the LNA due to its low noise and good gain at high frequency. These properties were confirmed using some measurement techniques including Probe, Oscilloscope and Network Analyzer for the simulation and practical testing of the amplifier to verify the performance of the designed High frequency Low noise amplifier. The design was able to fulfill the design goals of noise figure of < 1 dB, gain of 16.6 dB, Ic of 4.998mA and receiver sensitivity of -123.95dBm. A mathematical relationship has been derived relating the receiver's sensitivity to the channel capacity and noise figure of the device. The design specifications for this amplifier are in high demand following the recent developments in wireless technology.***

Keywords— ***Low Noise Amplifier (LNA), sensitivity, gain, high frequency.***

1. INTRODUCTION

1.1 BACKGROUND INFORMATION

Low Noise Amplifier (LNA) in today's communication system provides the first level of amplification of the signal received at the system's antenna. The smallest possible signal that can be received by the receiver defines the receiver's sensitivity. The largest signal that can be received by the receiver establishes an upper power level limit that can be handled by the system while preserving voice or data quality. The dynamic range of the receiver, which is the difference between the highest possible received signal level and the smallest possible received signal level, defines the quality of the receiver chain. The LNA function plays an undisputed importance in the receiver design. Its main function is to amplify extremely low signals without adding noise, thus preserving the required signal to noise ratio of the system at extremely low power levels. Additionally, for high signal levels, the LNA amplifies the received signal without introducing any distortions, hence eliminating channel interference. Due to complexity of the signals in today's digital communications, additional design considerations are usually addressed during an LNA design procedure. [5] Wireless communications are very lossy, so signals travelling from far away normally suffer from a lot of degradation. Hence, the LNA is located very close to the antenna; in fact the first component after the antenna is the low noise amplifier (LNA). An LNA is the combination of low noise, high gain and stability over the entire range of operating frequency.

2. METHODOLOGY

2.1 The design process

The design process started with studying available designs. Some relevant circuits are reproduced and simulated using available CAD tool (Multisim 11.0) to understand the engineering trade offs behind each design. For each of the design studied; noise sensitivity, gain, operating frequency were the focal parameters considered.

The design started with the direct current (DC) and alternating current (AC) analysis of the circuit topologies. Then the circuit was actualized in Multisim 11.0 and simulated to confirm the functionality performance of the circuit by measuring the stability factor, S-parameter, gain and operating frequency using virtual network analyzer. Thereafter, the layout of the design circuit schematic was developed using ultiboard layout software where the size of the design was adjusted and the placement of the components was arranged. An acid etching method was used to etch the board. This

involved the designed circuit schematic layout mirrored and printed on a glossy A4 paper using HP LaserJet professional M1212 series. The printed circuit schematic was cut out and placed on a Copper clad FR4 laminate 1.6 mm thick (35um copper) board which was cut to the size of the circuit layout which is 110mm x 60mm. An electronic iron is then used to imprint the schematic on the board by ironing the paper on the board for about fifteen minutes. It was put in a beaker of cold water for about fifteen minutes. The paper was removed. A copper board with PCB pads and signal lines traced out in black toner was obtained. The holes where the circuit components will be placed were drilled out using drilling machine. The Etching Ferric chloride solution, about 1 litre was prepared and the board was immersed and stirred for about five minutes. The board was removed and washed till all unnecessary copper is etched away from the board. The insulating drawing material used was removed by cleaning the board with cutting wool immersed in acetone solvents. Finally, the board was polished using polish remover (thinner) and this also preserve the board from eroding.
The designed low noise amplifier was tested using a signal generator and oscilloscope.

2.2 CIRCUIT DESIGN OF A HIGH FREQUENCY LOW NOISE AMPLIFIER

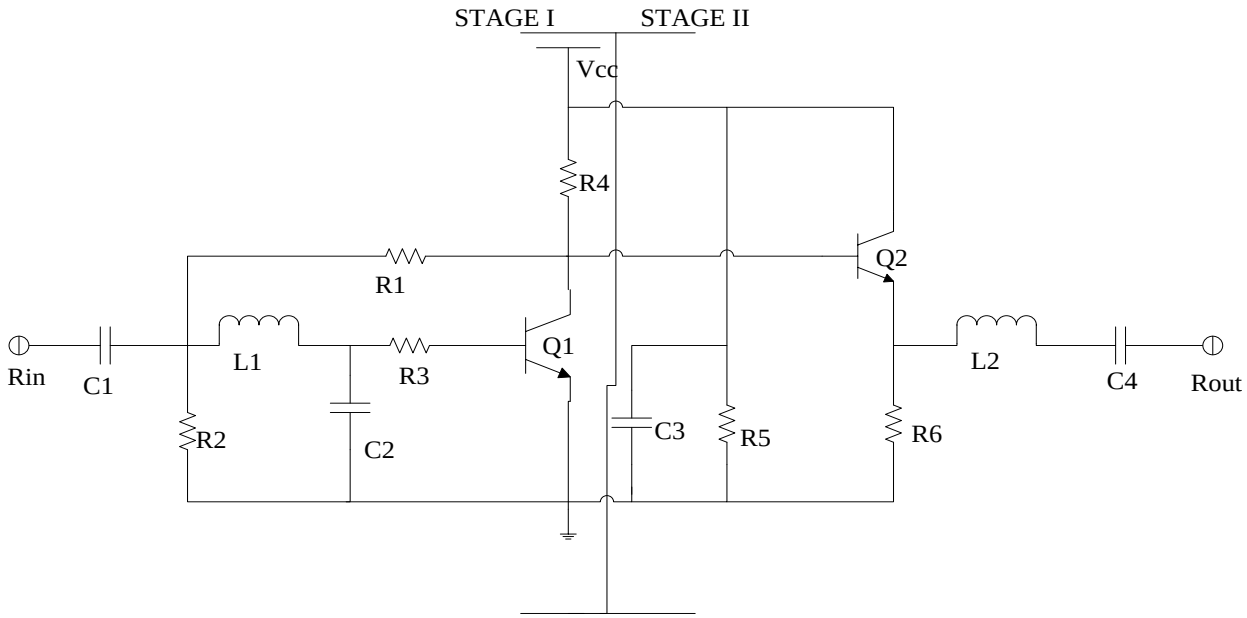

Fig 1: LNA Design

2.3 DC ANALYSIS OF THE LNA CIRCUIT

STAGE I

V_{BE} = 0.7V, β = 125; $V_{BB} = \left(\frac{R2}{R1+R2}\right)Vcc$ 2.1

Insert the values of R1 =$20 \times 10^3\Omega$, R2 =$20 \times 10^3\Omega$, R3 =10Ω, Vcc = 3V in equation 3.1

$$VBB = \left(\frac{20\times10^3}{20\times10^3+20\times10^3}\right)3 = 1.5V$$

Looking at a closed loop around Ib in the first stage transistor Q1

$VBB = IbR2 + IbR3 + VBE$ 2.2

$1.5 = 20 \times 10^3\ (\text{Ib}) + 10\ (\text{Ib}) + 0.7$

$Ib = \frac{1.5-0.7}{20\times10^3+10} = 3.998 \times 10^{-5}Amp$

$Ic1 = \beta Ib$ 2.3

$Ic1 = 125 \times 3.998 \times 10^{-5} = 4.998\ mAmp$ 2.4

$Ie = Ic + Ib$

$Ie = 4.998 \times 10^{-3} + 3.998 \times 10^{-5} = 5.03798mAmp$

$VR4 = Ic1 \times R4$ 2.5

$VR4 = 4.998 \times 10^{-3} \times 133 = 0.665V$

$Vcc = VR4 + Vce$ 2.6

$Vce = Vcc - VR4 = 3 - 0.665 = 2.34V$ 2.7

$$I_E = 5.0379mAmp, I_c = 4.998mAmp,\ Internal\ Signal\ Resistance\ (re_i^i = \frac{25mV}{I_E})$$

$$re_i^i = \frac{25mV}{5.0379mA} = 4.96\Omega;\ Input\ Resistance\ (\ r_\pi) = \beta r_{e^i} = 125 \times 4.96 \cong 620.3\Omega \quad 2.8$$

$$R_{B_i}\ //\ R_{B_2} = 20k//20k = \frac{20 \times 10^3 \times 20 \times 10^3}{20 \times 10^3 + 20 \times 10^3} = 10\ k\Omega \quad 2.9$$

$$X_{L_1} = 2\pi fL = 2\pi(2.2 \times 10^9)(2.7 \times 10^{-9}) = 37.32\Omega \quad 2.10$$

Input Impedance; $Z_{in} = (R_{B_i}\ //\ R_{B_2})//(X_{L_1} + R_{B_2} + \beta r_{e^i})$

$$Z_{in} = (10 \times 10^3)//(37.32 + 10 + 620.29) = \frac{10 \times 10^3 \times 667.6}{10 \times 10^3 + 667.6} = 625.82\Omega \quad 2.11$$

$$A_{v1} = \frac{-R_L}{r_{in}} = \frac{-133}{620.39} = -0.214$$

In decibel; 10log (0.214) = -6.6959dB

Note V_f is parallel to V_{cc} = 3V, R_5=R_f = 500Ω , R_L = R_4 =133

$$V_f = I_{cf} \times R_5 \quad 2.12$$

$$I_{cf} = \frac{3}{500} = 6mAmp$$

STAGE II

Taking a close Loop at the second amplifier stage;

$$Vce = Vbe + IeRe \quad 2.13$$

$$2.34 = 0.7 + Ie \times 200$$

$$Ie = \frac{2.34 - 0.7}{200} = 8.2mAmp$$

$$Ie = Ic + Ib = \beta Ib + Ib = 125 \times Ib + Ib = 126Ib \quad 2.14$$

$$8.2mAmp = 126Ib;\ Ib = \frac{8.2mAmp}{126} = 6.5 \times 10^{-5}Amp \quad 2.15$$

$$Ic = \beta Ib = 125 \times 6.5\ 10^{-5} = 8.13mAmp \quad 2.16$$

Total Current is $IcT = Ic1 + Icf + Ic2$ 2.17

$$IcT = 4.998mAmp + 6mAmp + 8.13mAmp = 19mAmp \quad 2.18$$

$$re_i^i = \frac{25mV}{8.2mA} = 3.049\Omega;\ \beta r_{e_i^i} = 125 \times 3.049 = 381\Omega \quad 2.19$$

$XL_2 = 2\pi f_L = 2\pi \times 2.2 \times 10^9 \times 2.7 \times 10^{-9} = 37.32\Omega$ 2.20

$r_o = X_{L2}\ //\ R_E = 37.32//200$ 2.21

$$r_{out} = \frac{37.32 \times 200}{37.32 + 200} = 31.45\Omega$$

$$A_v = -R_L = -31.45 \quad 2.22$$

In decibel = 10 log (31.45) = 14.98dB

VOLTAGE GAIN

$$A_v = A_{v_1} \times A_{v_2} = -0.26 \times -31.45 = 6.7303 \quad 2.23$$

IN DECIBEL

20log 6.7303 = 16.6dB 2.24

Output Third Order Intercept Point (IP3)

$$OIP3 = 10 * \log(V_{ce} * I_c * 5)\ [dBm] = 10 * \log(2.34 \times 4.998 \times 10^{-3} \times 5) = -12.33dBm$$

Input Third Order Intercept Point (IP3)

$$IIP3 = OIP3 - Gain[dBm] = -6.53 - 16.6 = -23.13dBm$$

S11 = 0.701; S12 = 0.024; S21 = 1.029; S22 = 0.749

$$\Delta = S_{11} * S_{22} - S_{21} * S_{12} = 0.701 * 0.749 - 1.029 * 0.024 = 0.50$$

$$K = \frac{1 - S_{11}^2 - S_{22}^2 + \Delta^2}{2(S_{21} * S_{12})} = \frac{1 - 0.701^2 - 0.749^2 + 0.50^2}{2(1.029 * 0.024)} = 4.0$$

Unconditionally stable at 2.2 Ghz (k>1)

2.4 AC ANALYSIS

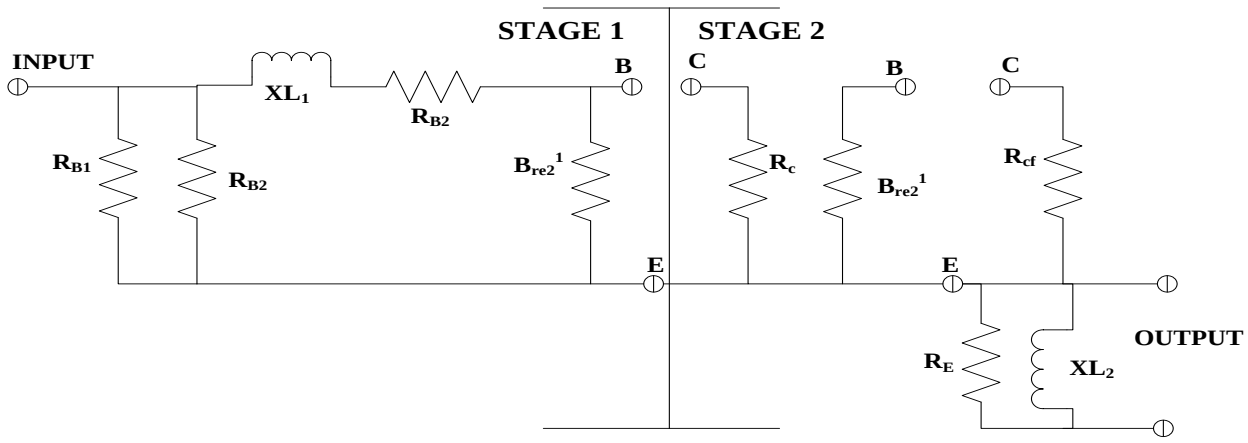

Fig 2: AC EQUIVALENT CIRCUIT FOR LNA DESIGN

2.5 AC EQUIVALENT CIRCUIT

STAGE 1

$re_i^i = \frac{25mV}{I_E}$ $I_E = 5.03798mAmp$, $I_C = 4.9$ ...mp, $C_\mu = 0.68$ pF

$$re_i^i = \frac{25mV}{5.03798mA} = 4.96\Omega$$

$$Transconductance(g) = \frac{I_E}{V_T} = \frac{5.03798mA}{25mV} = 0.2 \quad (2.25)$$

$$\text{Input Resistance } (r_\pi) = \beta r_{e^i} = 125 \times 4.96 \cong 620\Omega \quad (2.26)$$

$$C_\pi = \frac{g_m}{2\pi f_T} - C_\mu \quad (2.27)$$

$$C_\pi = \frac{0.2}{2\pi \times 2.2 \times 10^9} - 0.68 \times 10^{-12} = 1.38 \times 10^{-11} = 13.8\text{pF} \quad (2.28)$$

STAGE II

$I_c = 8.13mAmp$, $I_e = 8.2mAmp$, $C_\mu = 0.68$ pF

$$Transconductance(g) = \frac{I_E}{V_T} = \frac{8.2mA}{25mV} = 0.328$$

$$re_2^i = \frac{25mV}{I_E} = \frac{25 \times 10^{-3}}{8.2 \times 10^{-3}} = 3.049\Omega$$

$$\beta r_{e_i^i} = 125 \times 3.049 = 381.098 \quad (2.29)$$

$r_o = X_{L2} // R_E = 37.32//200$

$$r_{out} = \frac{37.32 \times 200}{37.32+200} = 31.45\Omega \quad (2.30)$$

$$C_\pi = \frac{g_m}{2\pi f_T} - C_\mu$$

$$C_\pi = \frac{0.328}{2\pi \times 2.2 \times 10^9} - 0.68 \times 10^{-12} = 2.3 \times 10^{-11} = 23\text{pF}$$

AT C1

The input resistance at C_1 is 620.29Ω from equation 3.26;

Hence the $R_{c1} = \frac{1}{10} of\ 620.29 = \frac{1}{10} \times 620.29 = 62.029\Omega$ (2.31)

$$C_1 = \frac{1}{2\pi R_{c1} F} = \frac{1}{2\pi \times 62.029 \times 2.2 \times 10^9} = 1.2pF \quad 2.32$$

AT C2

The input resistance at C_2 is 620.29Ω from equation 3.26;

Hence the $R_{c2} = \frac{1}{10} of\ 620.29 = \frac{1}{10} \times 620.29 = 62.029\Omega$

$$C_2 = \frac{1}{2\pi R_{c2} F} = \frac{1}{2\pi \times 62.029 \times 2.2 \times 10^9} = 1.2pF$$

AT C3

The resistance at C_3 is 500Ω;

Hence the $R_{c3} = \frac{1}{10} of\ 500 = \frac{1}{10} \times 500 = 50\Omega$

$$C_3 = \frac{1}{2\pi R_{c3} F} = \frac{1}{2\pi \times 50 \times 2.2 \times 10^9} = 1.45pF$$

AT C4

The resistance at C_4 is 31.45Ω from equation 3.30;

Hence the $R_{c4} = \frac{1}{10} of\ 31.45 = \frac{1}{10} \times 31.45 = 3.145\Omega$

$$C_4 = \frac{1}{2\pi R_{c4} F} = \frac{1}{2\pi \times 3.145 \times 2.2 \times 10^9} = 23pF$$

2.6 HIGHER FREQUENCY BOARDER FOR COUPLING AND BYPASS CAPACITOR

The critical frequency (f_c) for the circuit is the frequency that produces a capacitive reactance that is equal to the total resistance in the circuit (X_c=R). We know that the coupling capacitor acts as a short at high frequency but what does high mean, it means that 10times as high as the critical frequency (f_H>10f_c). A capacitor is an AC short at High frequency; a capacitor is a DC open at low frequency while an inductor is an AC open at High frequency; an inductor is a DC short at low frequency.

$$f_c = \frac{1}{2\pi Rc}; \quad 2.33$$

(a) At 2.3pf; the input resistance at C_1 is 620.29Ω from equation 3.26

$f_c = \frac{1}{2\pi(620.29)\times(2.3\times 10^{-12})} = 112\text{MHz}$

$f_H = 10f_c = 10 \text{ x } 112\text{MHz} = 1.12\text{Ghz}$ 2.34

As long as the generator (2.2GHz) is higher than 1.12Ghz; the capacitor act as AC short

(b) At 2.3pf; the input resistance at C_1 is 620.29Ω from equation 3.26

$f_c = \frac{1}{2\pi(620.29)\times(2.3\times 10^{-12})} = 112\text{MHz}$

$f_H = 10f_c = 10 \text{ x } 112\text{MHz} = 1.12\text{Ghz}$

As long as the generator (2.2GHz) is higher than 1.12Ghz; the capacitor act as AC short

(c) At 1.45pf; R=500Ω; $f_c = \frac{1}{2\pi(500)(1.45\times 10^{-12})} = 220\text{MHz}$

$f_H = 10f_c = 10 \text{ x } 220\text{MHz} = 2.2\text{Ghz}$

Since the generator (2.2GHz) is equivalent to 2.2GHz; the capacitor acts as AC open

(d) At 23pf; the resistance at C_4 is 31.45Ω from equation 3.30;

$f_c = \frac{1}{2\pi Rc} = \frac{1}{2\pi(31.45)(23\times 10^{-12})} = 220\text{Mhz}$

$f_H = 10f_c = 10 \times 220\text{MHz} = 2.2\text{Ghz}$

Since the generator (2.2GHz) is equal to 2.2 Ghz; the capacitor act as AC open

2.7 THERMAL NOISE

Thermal noise voltage across a resistor from equation 2.10 where the R is the input resistance and f the operating frequency is given by, [2].

$$V_t = \sqrt{4KTR\Delta f} = \sqrt{4 \times 1.38 \times 10^{-23} \times 300 \times 620.29 \times 2.2 \times 10^9} = \sqrt{2.26} \times 10^{-8} = 1.5 \times 10^{-4} V$$

2.8 LNA SENSITIVITY

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{G_1 G_2 \ldots\ldots G_N!}$$ [4].

F_1 is the thermal noise generated at the input resistance

$$F_1 = 10\log(1.5 \times 10^{-4} V) = 10 \times -3.824 = -38.24\text{dB}$$

F_2 is the noise generated at the first stage transistor which is 2.1dB from the datasheet

F_3 is the noise generated at the second stage transistor which is 2.1dB from the datasheet

F_4 is the thermal noise generated at the output resistance

$$F_4 = 10\log(3.464 \times 10^{-5} V) = 10 \times -4.46 = -44.6\text{dB}$$

$$F = -38.24 + \frac{2.1 - 1}{-6.69589} + \frac{2.1 - 1}{-6.69589 \times 14.97} + \frac{-44.6 - 1}{-6.69589 \times 14.97 \times 16.6} = -38.39\text{dB}$$

$$R_x\_Sen(dBm) = -174 + 10logBW + SNR + F$$ [3].

Assuming from the Nomograph of signal – noise ratio (SNR) as a function of probability of detection is at 98% which is equivalent to 12dB

Quality factor (Q) = $\frac{F_0}{BW}$ 2.35

A good signal quality factor varies from 10 – 50. Hence, assuming for a good signal quality to be 50 for this design.

BW = $\frac{2.2 \times 10^9}{50}$ = 44 Mhz

$$R_x\_Sen(dBm) = -174 + 10\log(44 \times 10^6) + 12\text{dB} + (-38.39\text{dB}) = -123.95\text{dBm}$$ 2.36

3. RESULTS

The result derived after simulating the circuits on MULTISM 11.0 which has been proven mathematically in the methodology that the circuit design can be used for the design of a high frequency low noise amplifier.

3.1 Simulation Result on Multisim 11.0

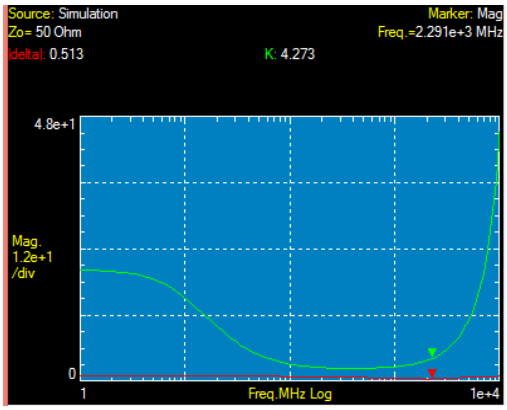

Fig 3: Multisim simulation of LNA Design stability

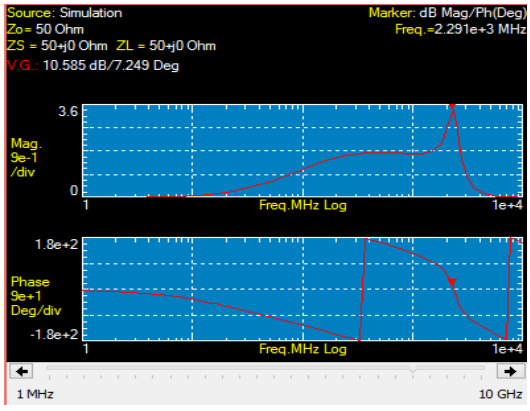

Fig 4: Multisim simulation of LNA Design Gain

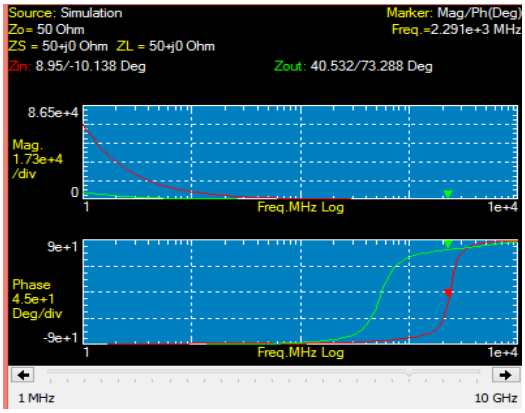

Fig 5: Multisim simulation of LNA Design input and output impedance

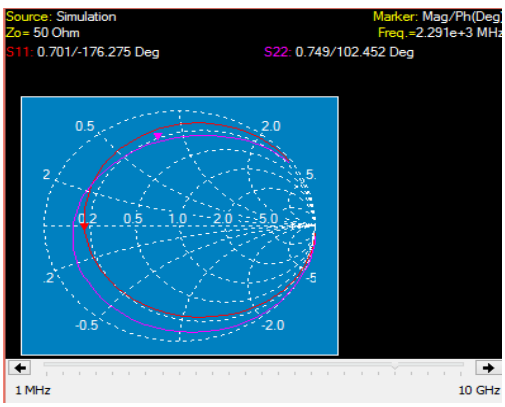

Fig 6: Multisim simulation of LNA Design S-Parameter

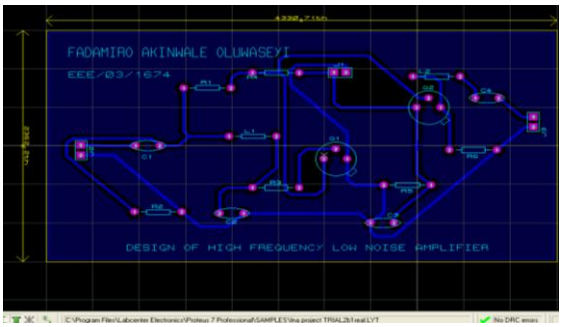

Fig 7: PCB layout for LNA design

Fig 8: PCB Board layout for LNA design

Table 1: DC parameters

AT FREQUECY 2.2GHz	SIMULATION	CALCULATION
GAIN	10.59dB	16.6dB
I_c	4.73mA	4.998mA
V_s	3V	3V
V_{ce}	2.37V	2.34V
Sensitivity		$-123.95dBm$

Table 2: Gain variation with frequency

FREQUENCY	STABILITY (K>1)	GAIN
1.9GHz	3.68	7.42dB
2.0GHz	3.95	9.16dB
2.2GHz	4.27	10.59dB
2.5GHz	4.66	8.28dB

To achieve a good gain and sensitive receiver, the following has been analyzed;
The maximum Power Transfer theorem predicts that the noise power delivered from a source to a matched load can be delivered as;
P = KTB = -174dBm/Hz (The reference noise level in a 1Hz, at room temperature) 3.1
Where;
K = Boltzman's Constant = 1.38×10^{-23}
T = 300K
B = Bandwidth
Receiver sensitivity (Rx) = -174 + 10logB + SNR + N.F 3.2
SNR = Signal to Noise ratio
N.F = Noise Figure

$$SNR = 10log\frac{S_i}{N_i} \text{ (dB)} \quad (3.3)$$

S_i = Input signal
N_i = Input noise

$$N.F = 10log\frac{S_i/N_i}{S_o/N_o} = 10log\frac{SNR_i}{SNR_o} \quad (3.4)$$

SNR_i = Input signal to noise ratio
SNR_o = Output signal to noise ratio
From Shannon – Hartley's theorem [1];

$$C = B\log_2(1+\frac{S_i}{N_i}) = \frac{1}{\log_{10}2}B\log_{10}(1+\frac{S_i}{N_i}) = 3.32B\log_{10}(1+\frac{S_i}{N_i}) \quad (3.5)$$

C = Channel capacity (bits/sec),
Making B the subject of the formula;

$$B = \frac{C}{3.32\log_{10}(1+\frac{S_i}{N_i})} \quad (3.6)$$

Substitute for equation 3.3, 3.4, 3.6 in equation 3.2

$$Rx = 10\log_{10}\frac{C}{3.32\log_{10}(1+\frac{S_i}{N_i})} + 10log\frac{S_i}{N_i} + 10log\frac{S_i/N_i}{S_o/N_o} - 174 \quad 3.7$$

Note $\log_{10} A + \log_{10} B = \log_{10} A \times B$ 3.8

$$Rx = 10\log_{10}\frac{C}{3.32\log_{10}(1\times\frac{S_i}{N_i})} \times 10log\frac{S_i}{N_i} \times 10log\frac{S_i/N_i}{S_o/N_o} - 174 \quad 3.9$$

$$Rx = 10\log_{10}\{\frac{C}{3.32\log_{10}(1\times\frac{S_i}{N_i})} \times \frac{S_i}{N_i} \times \frac{S_i/N_i}{S_o/N_o}\} - 174$$

$$Rx = 10\frac{C}{3.32} \times \frac{S_i/N_i}{S_o/N_o} - 174 = 3.012 \times C \times \frac{S_i/N_i}{S_o/N_o} - 174 \quad 3.10$$

Rx = 3.012CN.F – 174 3.11

Hence, it has been derived and concluded that the two major trade off for a high level of receiver sensitivity is the channel capacity and noise figure.

4. DISCUSSION

The design of an LNA for a wireless mode of operation at a high frequency range of 2.0 GHz - 2.5 GHz with a good gain is determined majorly by the quality of RF transistor used in the design. The mode of operation of the LNA design has been analyzed with probe, Network Analyzer and oscilloscope in Multisim 11.0

During the simulation and parameter swiping, it was discovered that the capacitor C1 and C2 have a large influence on the gain and the impedance on the design which is the tradeoff. At C1 and C2 which equals to 1.2pF, the gain is about 1dB which is very low but the input and output impedance are 32 Ω and 40 Ω respectively. But when the values of C1 and C2 where varied to 2.3pf, the gain of the design was approximately 10.8dB while the input and output impedance are 10Ω and 40Ω respectively. While both capacitor where varied to get a better gain and impedance value, it was discovered that the system becomes unstable and unreliable. Hence, the tradeoff in this design is now base on getting a better gain than an input impedance.

The DC analysis of the LNA design was properly analyze to get a proper biasing and a minimal base current. The AC analysis was carefully analyzed following the parametric components in the design to ensure the design can adequately work in the design frequency. The gain and the noise generated which are very essential in LNA design are analyzed carefully so that adequate signal propagation can be received with minimal signal to noise ratio.

The results derived after simulation using multisim 11.0 are shown in fig 3, fig 4, fig 5 and fig 6 and calculated results are shown in eq 2.4,eq 2.7,eq 2.11, eq 2.20, eq 2.23 and eq 2.36. While the PCB design has been shown in fig 7 and fig 8. Various mathematical relationship has been studied and analyzed. Hence, a mathematical relationship between Shannon's Hartley, quality factor, Boltzmann's constant, room temperature, signal to noise ratio and noise figure of the system was studied. A mathematical equation was derived which now relates the sensitivity of the LNA to the channel capacity and the noise figure as show in equation 3.11.

Both the simulated and calculated results were compared on table 1. This design was based on 50 Ω input and output impedance considering the fact that most RF designs are designed to be 50Ω.

The design of a high frequency, high gain and high sensitive low noise amplifier which can be used in various wireless devices at the range of 1.8 – 2.5 Ghz has been fabricated to suit the desired frequency range with proper tradeoff been consider between the gain and the noise figure.

5. CONCLUSION

The design proposed is efficient in the wireless Communication applications for amplifying the wideband RF signals at 2.2GHz with a gain of 10.59dB, sensitivity of -123.95dBm and Low Noise Figure of -38.39dB. Some possible discrepancies are measurement errors by the reading, non-equality of the components and most importantly the simulating tool used (network analyzer). The design of a LNA in Radio Frequency (RF) circuit requires the trade-off many importance characteristics such as gain, Noise Figure (NF), stability, sensitivity, input and output impedance. This situation forces designers to make choices in the design of RF circuits. After simulating the design and some necessary tradeoff has been done which has already compromise the proposed design gain, input and output impedance and the noise factor; the design was now reproduced on PCB. The electrical characteristics of the printed circuit board (PCB) used to physically mount and connect the circuit components in the design of a high frequency LNA product does have a significant impact on the performance of that design as well. The potential magnitude of the effect of the PCB design

increases with frequency as the parasitic elements tend to a similar magnitude to the typical lumped components used. The high frequency and sensitive LNA has been design and produced on PCB. The size of the PCB circuit board is 110mm x 60mm.

6. REFERENCES

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