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Design and Simulation Study of Active Balun Circuits for WiMAX Applications

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ABSTRACT— ***The paper presents a design and simulation study of three active balun circuits implemented in a standard 90nm Complementary Metal-Oxide Semiconductor (CMOS) process namely: (1) common-source/drain active balun; (2) common-gate with common-source active balun; and (3) differential active balun. The active balun designs are intended for Worldwide Interoperability for Microwave Access (WiMAX) applications operating at frequency 5.8GHz and with supply voltage of 1V. Measurements are taken for parameters such as gain difference, phase difference, and noise figure. All designs achieved gain difference of less than 0.23dB, phase difference of 180° ± 7.1°, and noise figure of 7.2–9.85dB, which are comparable to previous designs and researches. Low power consumption attained at the most 4.45mW.***

Keywords— Active balun; WiMAX; gain difference; phase difference

1. INTRODUCTION

The Radio Frequency (RF) front-end of a wireless receiver is of particular interest to many researchers and RF Integrated Circuit (RFIC) designers as it proves to be the most critical part in many communication systems and wireless applications such as Bluetooth, Wireless Fidelity (WiFi), and Worldwide Interoperability for Microwave Access (WiMAX). The block diagram of a typical receiver is shown in Figure 1.

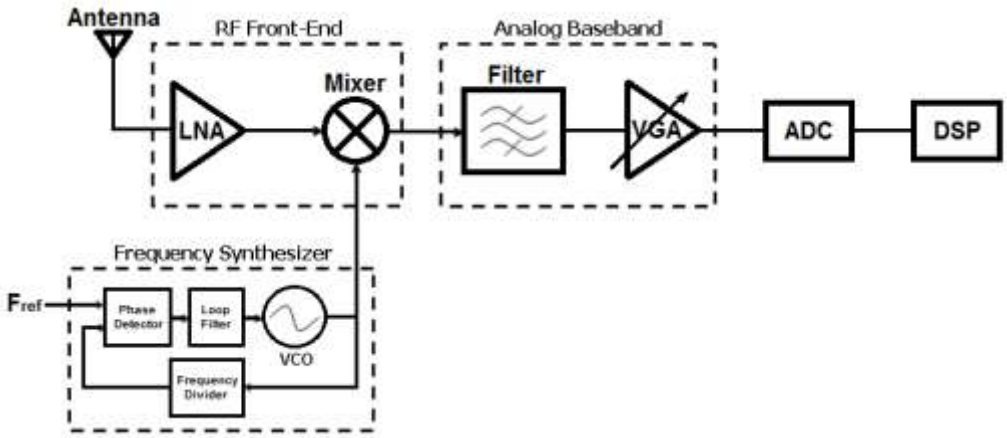


Figure 1: Block diagram of a typical wireless receiver

Some of RF front-end circuits are often designed as differential circuits. Fully differential approach is usually preferred in RFIC design due to its advantages, particularly the high immunity to common-mode noises, rejection to parasitic couplings, and increased dynamic range [1] [2]. Now, in order to supply input signal to differential circuits, a building block capable of supplying balanced differential signals is needed without sacrificing the performance of the overall system in terms of gain, noise figure, and linearity. Active balun (balanced-unbalanced) is capable to perform the necessary tasks.

Balun circuit is a type of transformer that converts signals that are single-ended or unbalanced with respect to ground

into signals that are differential or balanced with respect to ground, and vice versa. Baluns can be classified as either active or passive baluns depending on the devices used. Active baluns, although unidirectional and more complex to implement, are preferred over their passive counterparts because they can produce gain, occupy less chip area and can operate at higher frequencies [1].

2. ACTIVE BALUN DESIGN

Active balun circuit can be used as the first block of the WiMAX receiver front-end to supply differential signal to a differential low-noise amplifier (LNA) as shown in Figure 2. It can also be used to supply differential signal to a mixer, as illustrated in Figure 3. Figure 4 shows the active balun circuit as an intermediate block between the LNA and the mixer. Note that the configuration depends on the gain, noise figure (NF), and linearity requirements of the system. Since LNA is the first block in the receiver front end, it is critically designed with high gain of at least 25dB and noise figure of less than 2dB. Based on past researches, active balun has relatively high noise figure and lower gain performance compared to LNA, hence cannot be considered as the first block in the receiver front-end. Ultimately, the challenge is to design an active balun as an intermediate block to allow the LNA's output to connect with a differential mixer's input, with performance conforming to the requirement for the WiMAX receiver front-end.

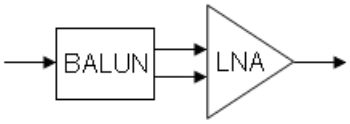


Figure 2: Active balun supplying the LNA

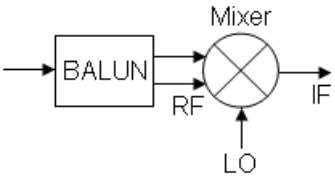


Figure 3: Active balun supplying the mixer

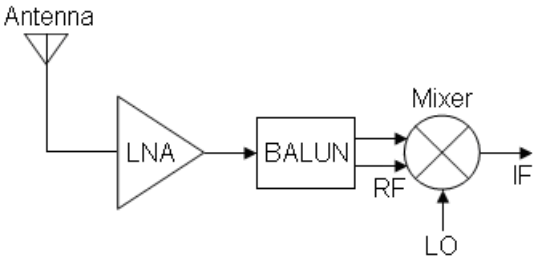


Figure 4: Active balun as intermediate block between LNA and mixer

In this research paper, three active balun circuits are designed and implemented in a standard 90nm Complementary Metal-Oxide Semiconductor (CMOS) process namely: common-source/drain, common-gate with common-source, and differential active baluns. The supply voltage (Vdd) for all the active balun designs is set to 1V. The lengths (L) of all transistors are set to 100nm, which is the minimum allowed channel length for the technology used. Transistor widths (W) are carefully computed to ensure the operation of all the transistors at saturation.

As mentioned earlier, the paper deals with the design of active baluns as intermediate block between LNA and mixer in the WiMAX receiver front-end. Table 1 summarizes the target specifications of the active balun design. These values are based from past active balun researches and from the summary of parameters as per WiMAX standard [3].

Table 1: Minimum target specifications for active balun design

Parameters	Value
Frequency	5.8GHz
Gain difference	< 1dB
Phase difference	180° ± 10°
Noise figure	< 10dB
Power consumption	< 10mW

Two most important parameters of the active balun are the gain difference and phase difference. Gain difference is the difference of the gains from the two output nodes of the active balun while the phase difference is the difference between the phase of the non-inverting output node RFout1 and the phase of inverting output node RFout2 of the active balun. Noise figure on the other hand, is the measure of the amount signal-to-noise-ratio (SNR) degradation introduced by the circuit as seen in the output.

2.1 Common-Source/Drain Active Balun

The common-source/drain is the simplest balun topology as it is composed of a single transistor M1 only as shown in Figure 5. The input signal is fed into the gate of the transistor. Normal operation results in an inverted output signal at RFout2 and a non-inverted signal at RFout1. Ideally, these two outputs would have the same amplitude with a phase difference of 180º. Load resistors R1 and R2 determine the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

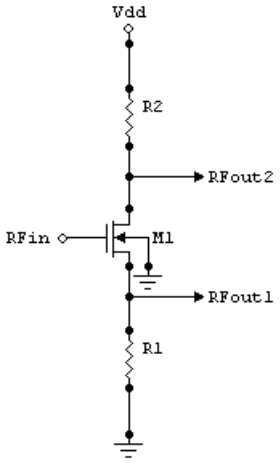


Figure 5: Common-source/drain active balun schematic

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. Common-drain topology or source-follower, on the other hand, is occasionally employed as level shifters or buffers, impacting the overall frequency response. It also exhibits high input impedance. With the two topologies merged to function as an active balun, common-drain will dominate the response on the overall voltage gain or attenuation because of the feedback effect of load resistor R1 with respect to the input.

2.2 Common-Gate with Common-Source Active Balun

This active balun is comprised of 2 amplifiers namely common-gate amplifier M1 in the 1st stage and common-source amplifier M2 in the 2nd stage as shown in the Figure 6. The input signal is fed into the drain of M1 and into the gate of M2, while the outputs are probed at the drains of M1 and M2. Load resistors R1 and R2 dictate the output voltages as well as the voltage gains of the two output signals with respect to the input signal. .

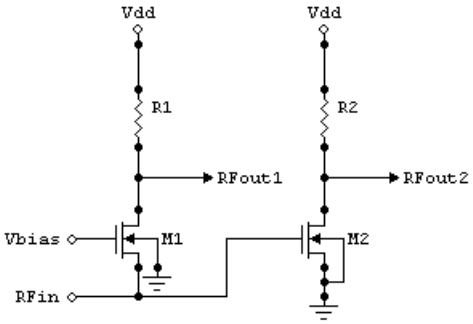


Figure 6: Common-gate with common-source active balun schematic

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. With this, it finds wide application in analog circuits and its frequency response is of interest. Common-gate topology exhibits no Miller multiplication of capacitances, potentially achieving a wide band [4]. However, the low input impedance may load the preceding stage. Furthermore, since the voltage drop across R1 is typically maximized to obtain the required gain, the DC level of the input signal must be quite low. With the two topologies connected as such to function as an active balun, one major challenge would be to generate balanced gain for the two outputs RFout1 and RFout2 with respect to the input signal RFin, given that the input signal is fed into two different transistor ports.

2.3 Differential Active Balun

The differential active balun, as shown in Figure 7 is composed of 3 transistors namely M1 and M2 for the differential output, and M3 for the tail current. The input signal is applied at the input of one of the differential pair transistors and will ideally split equally between the pair with same amplitude and 180° phase shift. Just like the common-gate with common-source active balun, this active balun topology is capable of producing gain.

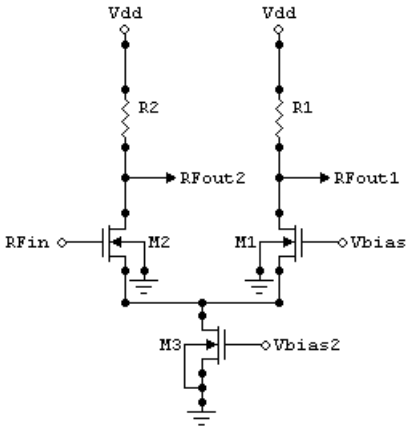


Figure 7: Differential active balun schematic

Differential active balun design follows the same design flow as the two previous active balun designs. With supply voltage Vdd set to 1V, branch currents flowing through M1 and M2 set the desired transistor dimensions to satisfy the performance parameters of the active balun, ensuring the allowed total power consumption. However, the impedance of M3 which acts as a current source is not as high as required because of non-ideality caused by parasitics at high frequency. This results in unequal signal distribution, hence affecting the gain balance and phase difference of the circuit. To mitigate this imbalance with transistor dimensions set identical for the branch transistors M1 and M2, adjustments are done at output loads R1 and R2.

2.4 Active Balun Design Summary

Three active balun designs are presented, namely common-source/drain active balun, common-gate with common-source active balun, and differential active balun. These active balun designs are optimized to meet the target performance specifications suitable for WIMAX receiver. All active designs are implemented in a standard 90nm CMOS process using Cadence Virtuoso software [5], a computer-aided design (CAD) tool and simulation software. Table 2 summarizes the active balun parameters.

Table 2: Active balun parameter expressions

Active Balun Parameter	Common-Source/Drain Active Balun	Common-Gate with Common-Source Active Balun	Differential Active Balun
Input bias voltage	0.8V	0.5V	0.8V
Output DC voltage for maximum swing	0.2V	0.75V	0.7V
	0.8V	0.55V	0.7V
Input impedance	∞	$1 / (g_{m1} + g_{mb1})$	∞
Output impedance, with resistor and capacitor loads	$R1 \parallel 1/sC1$	$R1 \parallel 1/sC1$	$R1 \parallel 1/sC1$
	$R2 \parallel 1/sC2$	$R2 \parallel 1/sC2$	$R2 \parallel 1/sC2$
Voltage gain, simplified (s = 0)	$\frac{g_m R1}{1+(g_m+g_{mb})R1}$	$\frac{(g_{m1}+g_{mb1})R1}{1+(g_{m1}+g_{mb1})Rs}$	$\frac{g_{m2}\cdot G_{m1}R1}{G_{m1}+G_{m2}+\frac{1}{R_{tail}}}$
	$\frac{-g_m R2}{1+(g_m+g_{mb})R1}$	$-g_{m2}R2$	$-\frac{(g_{m2}\cdot G_{m1}R2)+\left(g_{m2}\cdot\frac{R2}{R_{tail}}\right)}{G_{m1}+G_{m2}+\frac{1}{R_{tail}}}$
Noise figure	$10log\left[1+\frac{1+\gamma(g_m+g_{mb})R1}{C1\cdot k_B T\Delta f\cdot A_{v1}}\right]$	$10log\left[1+\frac{1+\gamma(g_{m1}+g_{mb1})R1}{C1\cdot 4\frac{1+\gamma g_{m1}R1}{(g_{m1}+g_{mb1})^2R1}\cdot A_{v1}}\right]$	$10log\left[1+\frac{1+\gamma(g_{m1}+g_{mb1})R1}{C1\cdot k_B T\Delta f\cdot A_{v1}}\right]$
	$10log\left[1+\frac{1+\gamma(g_m+g_{mb})R2}{C2\cdot k_B T\Delta f\cdot A_{v2}}\right]$	$10log\left[1+\frac{1+\gamma g_{m2}R2}{C2\cdot 4\frac{1+\gamma g_{m1}R1}{(g_{m1}+g_{mb1})^2R1}\cdot A_{v2}}\right]$	$10log\left[1+\frac{1+\gamma(g_{m2}+g_{mb2})R2}{C2\cdot k_B T\Delta f\cdot A_{v2}}\right]$

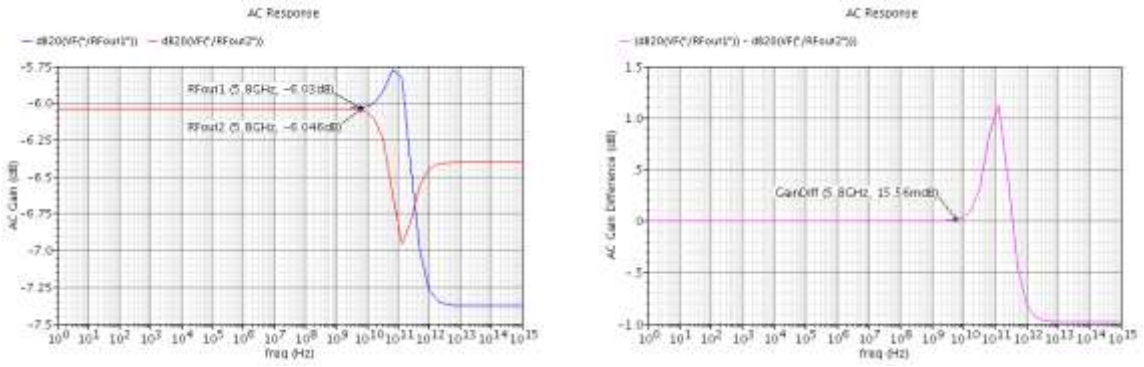
3. SIMULATION RESULTS AND ANALYSIS

All three active baluns are characterized and designed to achieve the target specifications. The extraction of all device parameters for use in simulations is done using Synopys Star-RCXT [6]. Simulations of the extracted view are done using Cadence Design Systems software. The active baluns are designed to operate at 5.8GHz, which is a typical frequency for WiMAX applications. Measurements in the simulation plots are taken at 5.8GHz.

3.1 Common-Source/Drain Active Balun

3.1.1 Gain and Gain Difference

AC (alternating current) analysis is used to determine the gains and gain difference of the two outputs with respect to the input at frequency of 5.8GHz, using ideal voltage source with input bias voltage V_{IN} set at 0.8V. Drain-to-source voltage, $V_{DS,Q} = V2 – V1$, was measured at 528.6mV with $V_{GS} – V_t = 71.6$mV, confirming the transistor M1 operating at saturation. Figure 8 shows the response using AC analysis.



(a) (b)

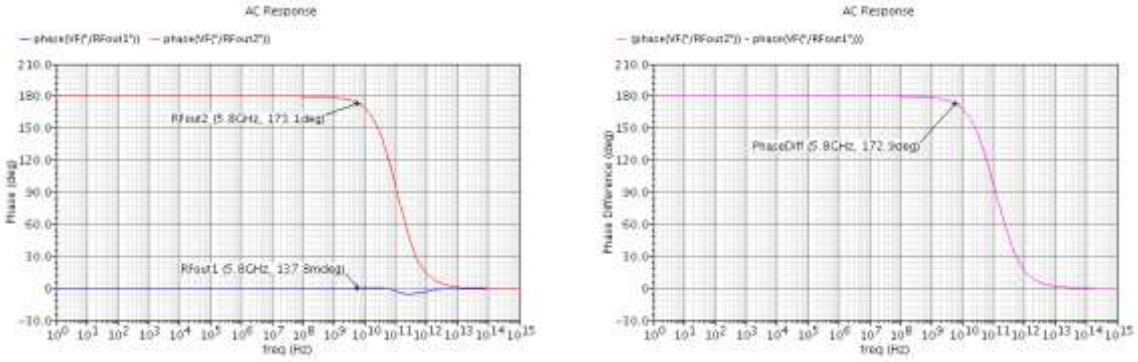
Figure 8: AC analysis, a) gains b) gain difference of common-source/drain active balun

Since the active balun has the configuration of common-drain, it is expected that the gains would fall below the target of at least 0dB. AC gains are at around -6dB. Take note that the three active baluns are designed with ideal voltage

source at the input, thus with very high (if not infinite) input impedance, and the output is left with no termination. Since the resistor loads of the active balun are of the same value, gain difference was maintained very low at 0.015dB.

3.1.2 Phase and Phase Difference

Figure 9 shows the phase and phase difference response using AC analysis, and using ideal input voltage source.



(a) (b)

Figure 9: AC analysis, a) phases b) phase difference of common-source/drain active balun

Same analysis with the gain and gain difference are done with the phase and phase difference. The results are within the acceptable values especially for the target phase difference with measurement at 172.9° using SP (S-parameter) analysis.

3.1.3 Noise Figure

PSS+PNoise (periodic steady state + periodic noise) analysis is done to measure the noise figure of the active balun. With this analysis, it is required to include input and output termination ports with 50Ω impedance. Figure 10 shows the noise figure generated using the said analysis.

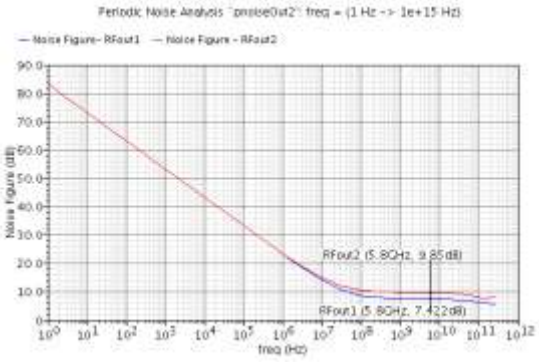


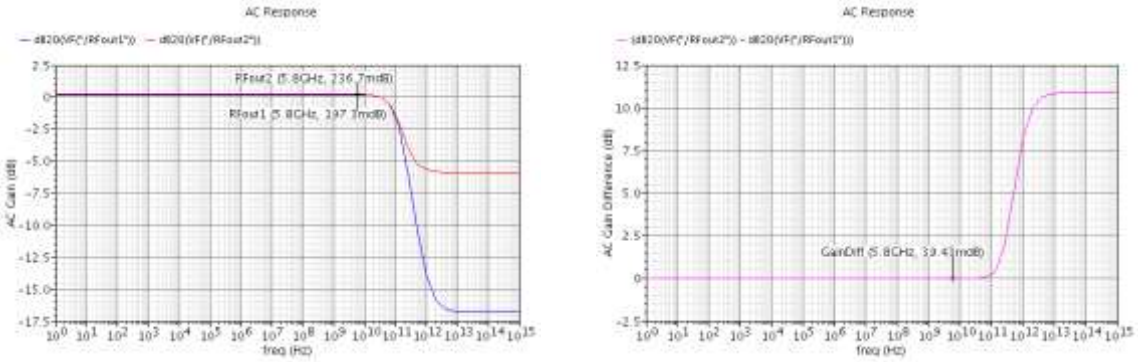
Figure 10: Noise figure of common-source/drain active balun

Noise figure of 7.422dB and 9.85dB for RFout1 and RFout2 with respect to RFin are generated using PSS+PNoise analysis with RF input power set to -20dBm. It is worth noting that the noise figure from PNoise analysis is slightly higher than the noise figure generated from SP analysis because at prf = -20dBm the active balun demonstrated very weak nonlinearity and noise as other high harmonics are convoluted [7] [8].

3.2 Common-Gate with Common-Source Active Balun

3.2.1 Gain and Gain Difference

Same setup is used for all active baluns as earlier presented in 3.1.1. Figure 11 shows the gain and gain difference using AC analysis. Input bias voltage V_{IN} is set at 0.45V. Both transistors M1 and M2 satisfied the requirements for saturation region condition.



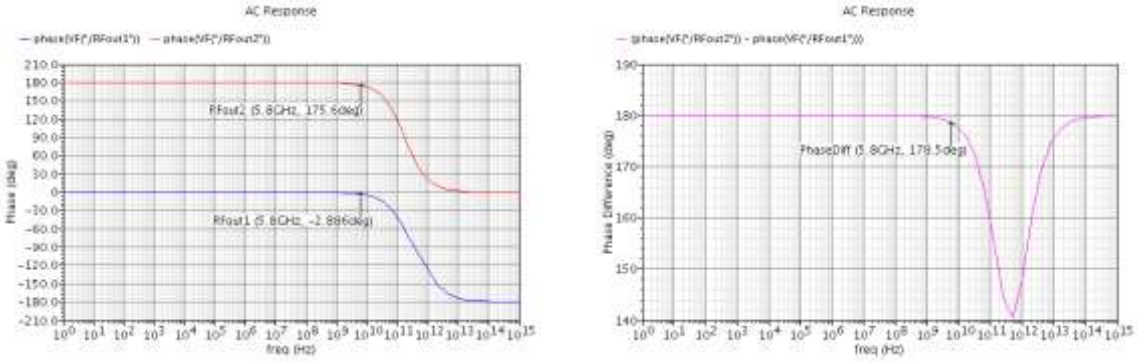
(a) (b)

Figure 11: AC analysis, a) gains b) gain difference of common-gate with common-source active balun

Common-gate with common-source active balun is designed to achieve a gain of just above 0dB. This is validated in the AC gain results in Figure 9-b. Gain difference is close to zero as expected since the gain response for the two outputs is very close to each other.

3.2.2 Phase and Phase Difference

Figure 12 shows the phase and phase difference response using AC analysis with ideal input voltage source.



(a) (b)

Figure 12: AC analysis, a) phases b) phase difference of common-gate with common-source active balun

The results are within the target specification for the phase difference. AC analysis measurement for phase difference is at 178.5° at 5.8GHz frequency of operation.

3.2.3 Noise Figure

Figure 13 shows the noise figure response using PSS+PNoise analysis.

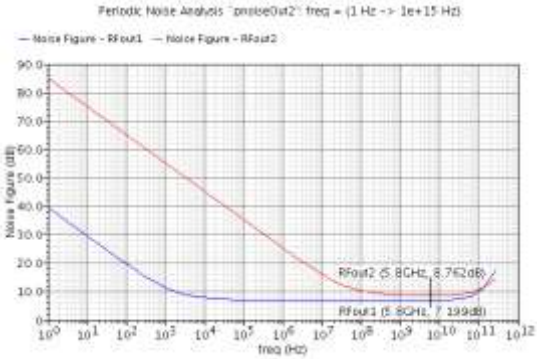


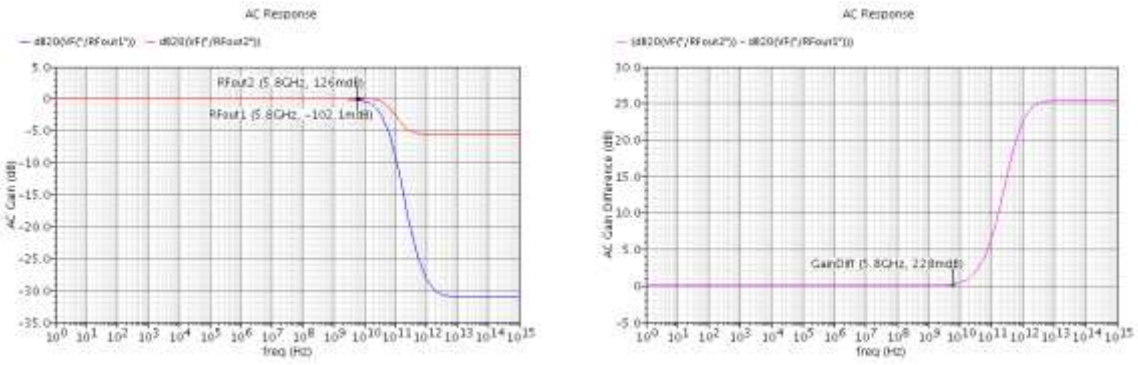
Figure 13: Noise figure of common-gate with common-source active balun

Noise figure of 7.199dB and 8.762dB for RFout1 and RFout2 with respect to RFin are generated using PSS+PNoise analysis taken at frequency of 5.8GHz. The values conformed to the noise figure requirement set for the active balun design.

3.3 Differential Active Balun

3.3.1 Gain and Gain Difference

Shown in Figure 14 are the gain and gain difference response using AC analysis. Ideal voltage source is used with input bias voltage V_{IN} set to 0.8V. All transistors M1, M2, and M3 are carefully derived and designed to satisfy the saturation region condition, with all $V_{DS,Q}$ at around 0.3V.



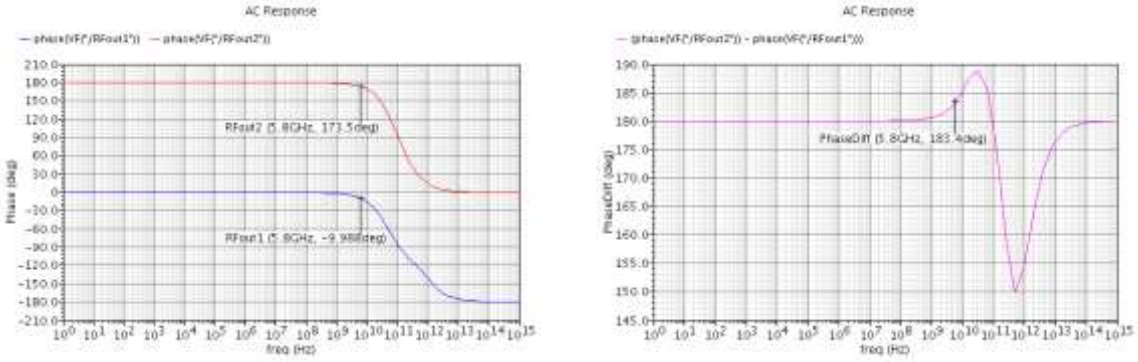
(a) (b)

Figure 14: AC analysis, a) gains b) gain difference of differential active balun

Differential active balun is designed to achieve a gain a little over 0dB. This is shown in the AC gain results in Figure 14-b. Gain difference at 5.8GHz is at 0.228dB, which is still close to zero as expected since the gain response for the two outputs is very close to each other. The active balun is designed using ideal voltage source and with relatively high resistor loads at 250Ω and 178Ω to satisfy the needed gain.

3.3.2 Phase and Phase Difference

Figure 15 shows the AC analysis phase and phase difference response, with ideal input voltage source.



(a) (b)

Figure 15: AC analysis, a) phases b) phase difference of differential active balun

The results are within the target specification for the phase difference. AC analysis measurement for phase difference is at 183.4°.

3.3.3 Noise Figure

Figure 16 shows the noise figure result using PSS+PNoise analysis.

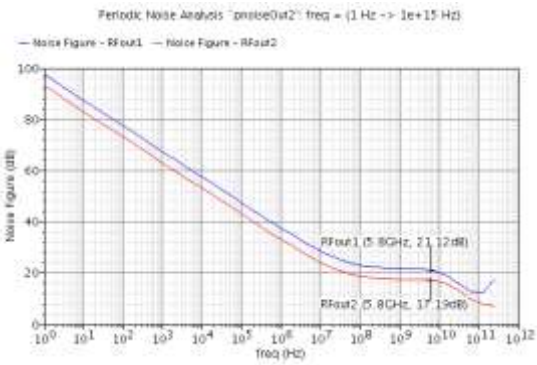


Figure 16: Noise figure of differential active balun

Noise figure of 21.12dB and 17.19dB for RFout1 and RFout2 with respect to RFin are generated using PSS+PNoise analysis with RF input power set to -20dBm. High noise figures are generated since very low output signals are produced due to affected output load setting. With output matching network introduced, noise figures were improved to 8.973dB and 9.781dB, respectively for the two outputs.

3.4 Results Summary

Table 3 summarizes the performance of the three active balun designs.

Table 3: Performance comparison of active balun designs

Parameter	Target Specification	Common-Source/Drain Active Balun	Common-Gate with Common-Source Active Balun	Differential Active Balun
Process/ Technology	90nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS
Supply voltage	1V	1V	1V	1V
Frequency	5.8GHz	5.8GHz	5.8GHz	5.8 GHz
Gain difference	< 1dB	0.016dB	0.040dB	0.228dB
Phase difference	180° ± 10°	172.9°	178.5°	183.4°
Noise figure	< 10dB	7.422dB 9.850dB	7.199dB 8.762dB	8.973dB 9.781dB
Power consumption	< 10mW	2.558mW	4.449mW	3.599mW

All active balun designs achieved a gain difference better than 1dB and a phase difference of 180°±10° or better at frequency of 5.8GHz. The active balun designs are affected with the input and output loading since these active baluns are designed with ideal input voltage source and no termination ports included. Low power consumption of at most 4.5mW is achieved, comparable to other low power designs in the past researches.

4. CONCLUSION AND RECOMMENDATIONS

Three active balun circuits are designed and implemented in a standard 90nm CMOS process namely common-source/drain, common-gate with common-source, and differential active baluns. These circuits are carefully designed to satisfy the WiMAX receiver requirement at 5.8GHz. Simulation measurements are taken for parameters such as gain, phase, gain difference, phase difference, and noise figure.

Because of its configuration, common-source/drain active balun could only produce voltage attenuation instead of gain. Input impedance of common-gate with common-source active balun is not that high compared to the other baluns, adding challenges to produce equal and balanced gain for the two outputs. Regardless, all designs achieved gain difference of less than 0.3dB and phase difference of 180° ± 7.1°. Noise figure performance is at around 7.2–9.85dB, comparable to previous designs and researches. Low power consumption of at most 4.45mW is achieved, comparable to other low power designs.

Future work could include designing active balun with high gain. Although it will sacrifice the bandwidth, it can still be realized at lower frequencies for practical applications. One possible work would be to integrate the active balun functionality on the circuit design of a differential circuit like that of the double-balanced mixer or differential LNA.

5. ACKNOWLEDGMENT

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