Package Design Optimization with Reliability Test Verification for Reduction of Voids and Delamination

Frederick Ray I. Gomez* and Rammil A. Seguido

New Product Introduction Department, Back-End Manufacturing & Technology, STMicroelectronics, Inc.
9 Mountain Drive, Light Industry & Science Park II, Brgy. La Mesa, Calamba City, Laguna, Philippines 4027

*Corresponding author's email: frederick-ray.gomez [AT] st.com

ABSTRACT— ***Package down-scaling or miniaturization has become the trend in semiconductor industry, with smaller and thinner package being the prime objective. Stacked dice process in semiconductor packages is now also becoming popular as semiconductor industries try to come up with products that offer multiple channels in a small IC (integrated circuit) package. However, as different dice are brought together, several challenges have to be overcome in terms of package design and assembly.***

This technical paper specifically considers the challenges encountered in the development of a compact and thinner package that incorporates multiple or stacked dice in one. For the case of this paper, Die1 is smaller than Die2 and must be the first one to be die bonded, making the internal construction an unbalanced stacked dice. Normally, stacked dice is in pyramid layout, wherein a single large die supports smaller top die. Nevertheless, success is measured when there is a solution to control die attach voids and eliminate or significantly minimize delamination for unbalanced stacked dice as mentioned. Ultimately, the paper presents the understanding of the factors involved and the package design optimization approach used to produce a successful unbalanced stacked die in a thin package using thin substrate.

Keywords— Semiconductor package; planarized; stacked dice

1. INTRODUCTION

The desire to combine several dice into a single molded IC (integrate circuit) package to get multiple desired functions has led to the development of multiple dice or stacked dice configuration of semiconductor package. Instead of separately mounting electronic components like analog ICs and digital ICs to the PCB (printed circuit board), they can now be integrated into a single package.

For this study, the internal construction of the semiconductor IC package or device (hereinafter referred to as Device S) must be designed to stack smaller Die1 (2.74 mm x 2.09 mm) at the bottom and larger Die2 (3.05 mm x 3.03 mm) on top, as illustrated in Fig. 1 and Fig. 2. An interposer silicon die (2.0 mm x 0.90 mm) was added to support the top die overhang in Fig. 2. The stacked dice were supported by 0.13mm substrate and molded with 0.42mm mold cap.

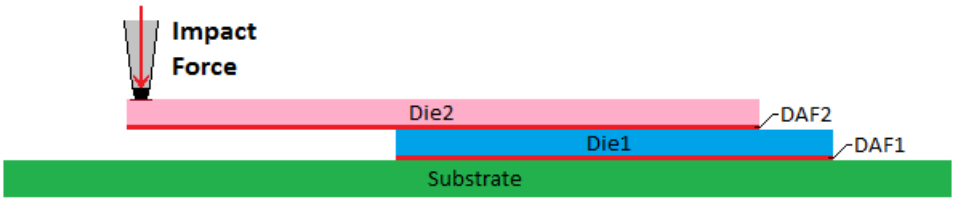


Figure 1: Cross-section of unbalanced stacked dice, affecting wirebonding

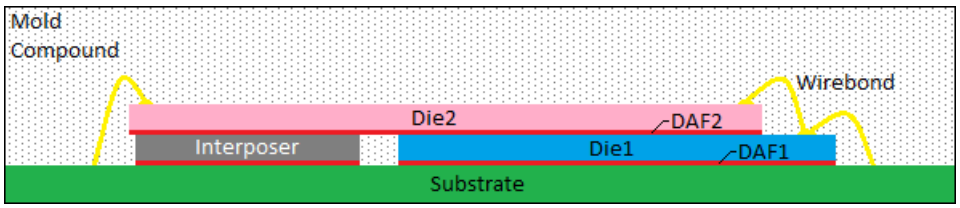


Figure 2: Package cross-section with interposer added to support Die2 (top die) overhang

Actual evaluation of the first version of Device S, conversely, showed that there were issues of delamination between Die1 (bottom die) and Die2 (top die). Also, die attach voids between Die1 and substrate were present. In order to address the issues encountered, factors involved in the delamination and voids were investigated and package design optimization focusing on substrate was carried out.

2. LITERATURE REVIEW

2.1 Stacked Dice Using Die Attach Film (DAF) on Substrates

Stacked dice robust die attach material is the Die Attach Film (DAF). Currently DAF has being widely applied on various high density packages such as BGA (ball grid array), CSP (chip-scale package), SIP (system-in-package), PoP (package on package) and other packages to its bleedless and consistent Bond Line Thickness (BLT) [1] [2] [3]. Typical assembly flow of BGAs includes dicing die attach film (DDAF), which integrates the die attach film and the dicing tape [1] [4] [5]. Traditional assembly flow with liquid-type die-attach material can be easily applied onto packaging with DAF. Process could be simplified by eliminating the dispensing and also skipping the post die attach cure. However, DAF void always is one of the major concerns, especially for its application between die and the substrate [6] [7]. Reliability issue of delamination likely occurs at the DAF-substrate interface [6] [8]. DAF void characteristics and its formation and reduction mechanism were then studied. Aside from die attach or diebonding parameters, many other factors are inevitable with regards to the void performance. For Device S, DAF voids between bottom dice (Die1 and interposer) and substrate were also considered as one of the contributors for the top die (Die2) delamination issue.

2.2 Substrate Package Construction

Substrate is normally constructed with metal planes to ensure Copper (Cu) balance and solder resist balance between layers to ensure no substrate delamination when subjected to reflow [8]. Electrical simulations in relation to the metal plane or metal strips in substrate should govern for resistance, inductance and capacitance. Fig. 3 shows the 2 layer (top side – M1 layer and bottom side - M2 layer) construction of the substrate for Device S, with metal balance of 16%.

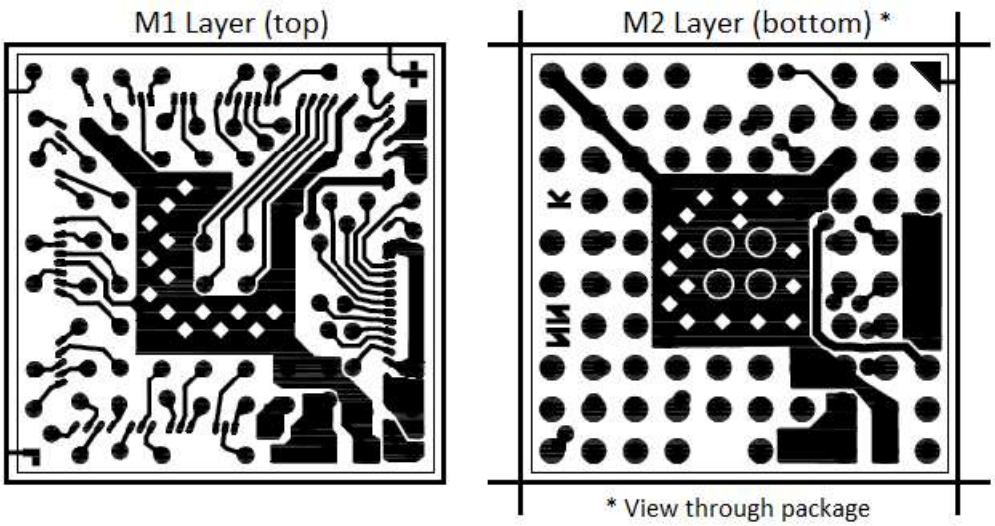


Figure 3: Top and bottom layers viewed through package

3. METHODOLOGY

3.1 Design Modification and Package Modeling

The first version of the Device S design created was using rigid and thin DAF (20um) for all stacked dice to ensure planarity in-between interfaces – 2 bottom dice to substrate and top die to the 2 bottom dice, and to ensure there is enough clearance for the wirebond looping after mold. Back-end assembly of Device S was performed (from die preparation to package singulation) and submitted samples for Moisture Sensitivity Level 3 (MSL3) to check for delamination. Reliability test showed top die delaminated from bottom dice and observed presence of DAF voids after cross-section validation. Fig. 4-5 shows the MSL3 results.

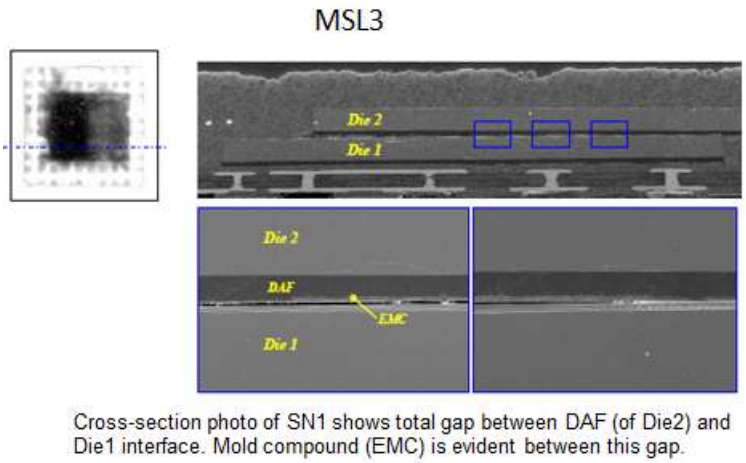


Figure 4: Die2 (top die) delamination

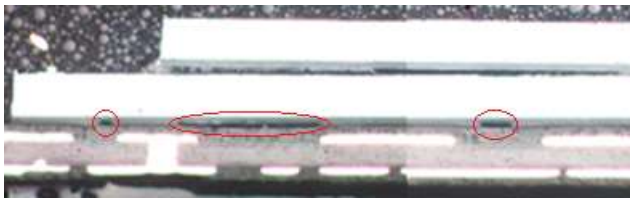


Figure 5: Die1 (bottom die) voids

With the results, a fault-tree analysis illustrated in Fig. 6 was then performed to prove the phenomenon that the ground plane expands after heat is applied.

Figure 6: Fault-tree analysis

3.2 Design Modification and Package Modeling

With the occurrence of voids between substrate and DAF interface with fixed pattern, affecting Die2 to delaminate, the substrate topography is mostly suspected. Fig. 7 shows that to identify the correlation between void and substrate surface, the cross section was further analyzed and found out that the metal plane expansion serves as fulcrum (not only as source of voids) thus affecting the planarity of 2 bottom dice which resulted to top die aggravated delamination. Therefore, the ground metal plane serves as peaks and solder mask as valleys.

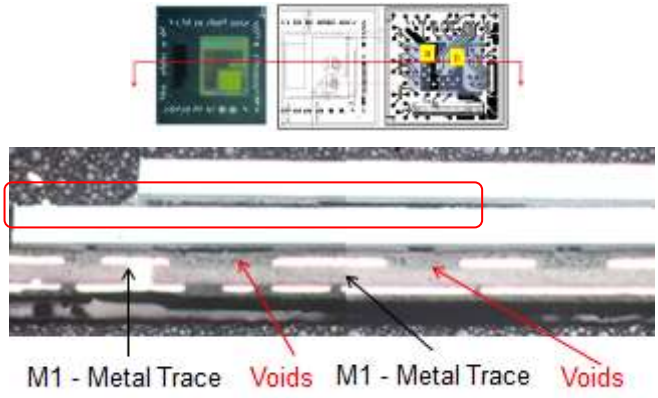
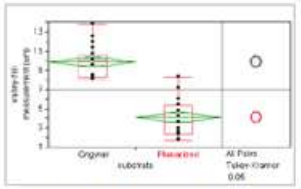


Figure 7: Metal trace of ground plane served as fulcrum and induced voids, thus Die2 delamination encountered

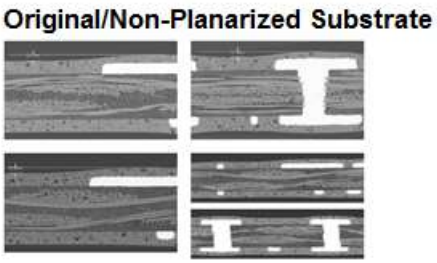
It can be checked that in every after metal plane, there is large void between die and substrate. Measurements of the peaks and valley were more than 10µm and DAF thickness is at 20µm. With this, DAF needs to fill the gap with depth equivalent with 50% of its thickness, which produces the challenge towards DAF gap filling capability. Therefore, these voids result from the insufficient gap and it can be explained that DAF voids have the properties of fixed position and similar pattern, which is matched with substrate surface topography. A comparison of the original or non-planarized substrate and the planarized substrate was performed to check the difference as shown in Fig. 8. Difference of more than 5 microns was observed.

	Original	Planarized
Minimum	8.02 um	1.75 um
Average	9.92 um	4.11 um
Maximum	13.70 um	8.33 um
StDev	1.564 um	1.814 um

Planarity measurements are vertical depths from highest plateau points relative to lowest valley point.



Statistically, significant difference is exhibited between the original/non-planarized and the planarized substrate.



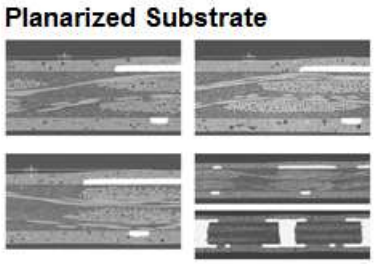


Figure 8: Non-Planarized vs. Planarized substrate comparison

3.3 Substrate Design Iterations

Considering the findings from the fault-tree analysis in Fig. 6, up to the cross-section verification in Fig. 7, the root-cause of Die2 delamination and voids between bottom dice (Die1 and interposer) and substrate is the substrate topography. Softer and thicker DAF for Die2 was considered to compensate variation of level of the two bottom dice. Table 1 was implemented to further validate the hypothesis using the existing materials in the production line.

Table 1: Process evaluation matrix

Evaluation Run #	DAF Evaluation	Substrate (with variation)	Remarks
1	Die2 and bottom dice – rigid and thin (20µm)	Non-planarized – existing for Device S	Control Run: Samples should fail MSL3 to validate the issue (with cross section validation)
2	Die2 – softer and thicker DAF (30µm), Bottom dice – rigid and thin (20µm)	Non-planarized – existing for Device S	Samples must pass MSL3 with cross section validation
3	Top die – softer and thicker DAF (30µm), Bottom dice – rigid and thin (20µm)	Planarized from other package	Response in time (0) with cross-section validation

4. RESULTS AND DISCUSSION

Package simulation results based on thermo-mechanical package modeling in Fig. 9 showed that warpage is relatively low. Actual package observation also confirmed the predicted low package warpage. Interface stress due to the Coefficient of Thermal Expansion (CTE) mismatch is also low, which implies that delamination could be due to other factors. Results of the package modeling exhibited low risk if DAF material adhesion is high.

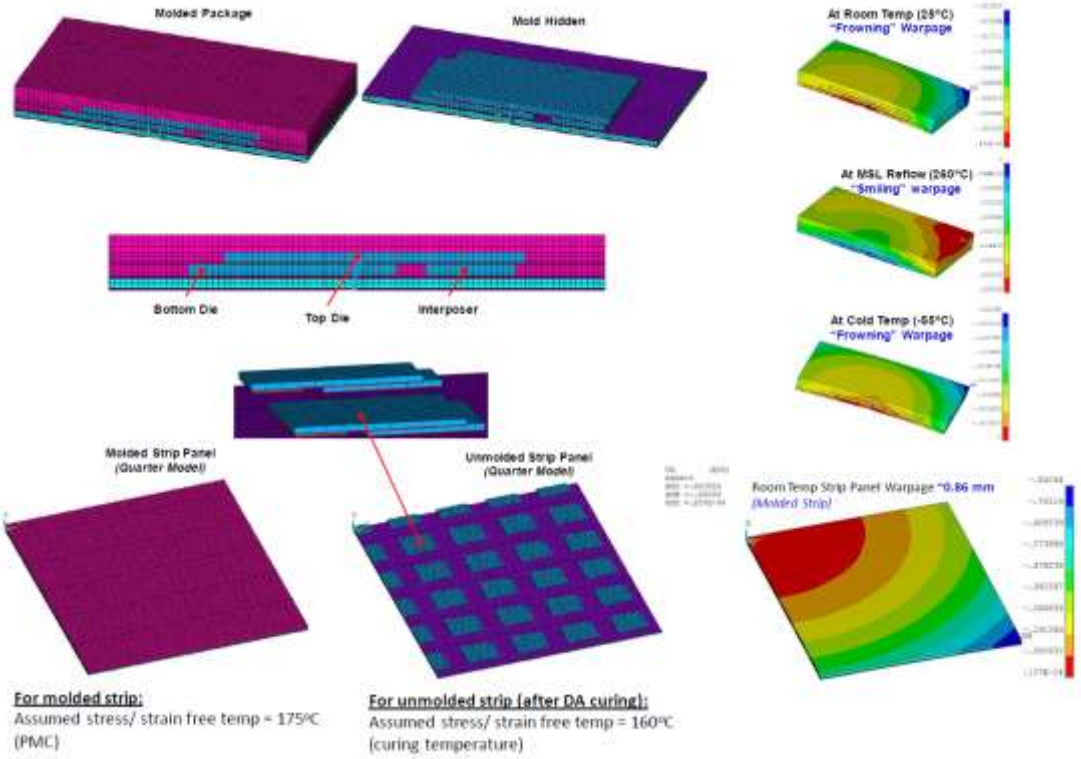


Figure 9: Device S thermo-mechanical simulations - package level and strip level

Reliability tests (MSL3) were done using a different DAF, this time softer and thicker DAF for Die2. Fig. 10 and 11 shows the MSL3 results.

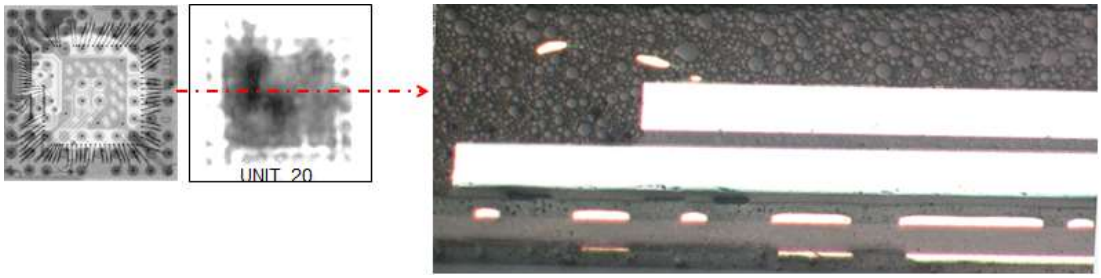


Figure 10: MSL3 passed on assembly package performed using softer and thicker DAF for Die2

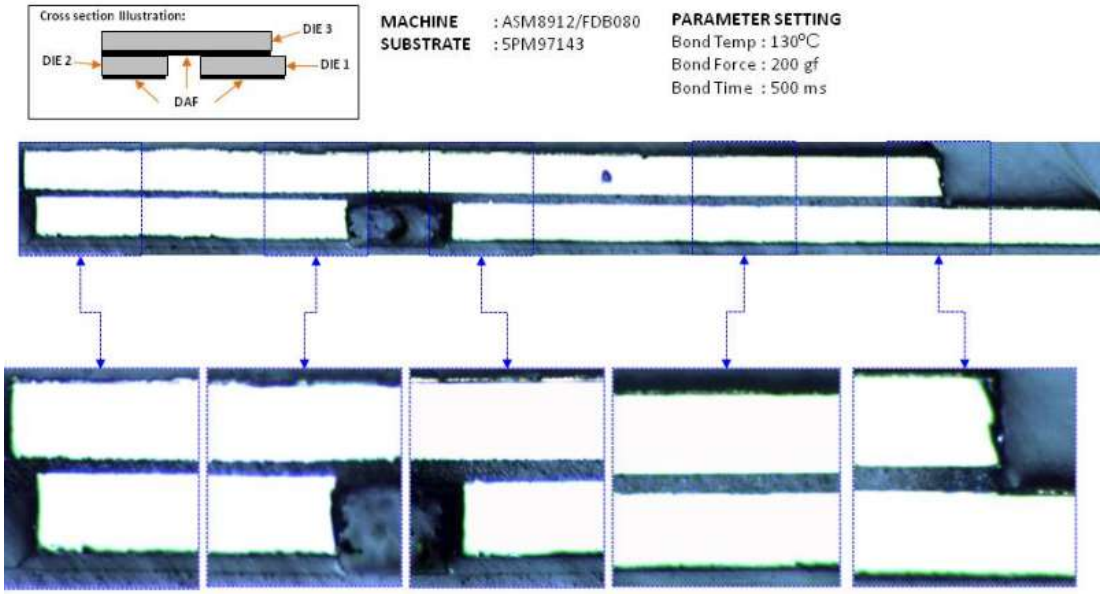


Figure 11: Die attach stacked dice using same rigid and thin DAF showed zero (0) voids for bottom dice at time zero (0)

Evaluation results are summarized in Table 2. Based on the results, Die2 should use softer and thicker DAF while bottom dice (Die1 and interposer) should use rigid and thinner DAF on a planarized substrate.

Table 2: Evaluation results summary

Evaluation Run #	Results	Remarks
1	Fail	Previous issue replicated
2	Pass	Passed MSL3
3	Pass	Passed die attach responses

5. CONCLUSIONS AND RECOMMENDATIONS

Based on the study with the three evaluation runs done, planarized substrate should be considered for DAF application. Die2 (top die) should use softer and thicker DAF to compensate variation of bottom dice. On the other hand, bottom dice (Die1 and interposer) should use rigid and thinner DAF to maintain level.

New substrate design for Device S proposal is shown in Fig. 12, replacing the metal plane in M1 with strip type metals and reducing M2 density resulted to better Cu balance [9]. Fig. 13-15 showed no significant difference in package electrical modeling performance for resistance, self-inductance and self-capacitance.

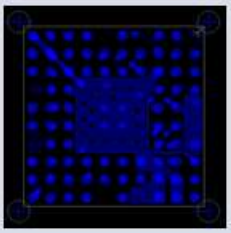
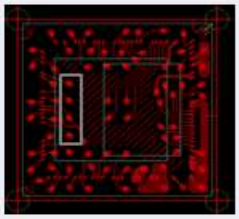
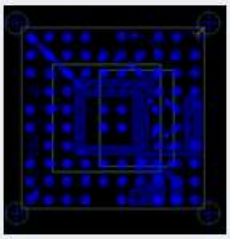
2-Layer, 0.13mm	M1: Top Layer	M2: Bottom Layer	Cu Balance
Non-Planarized (Original design)			16%
Planarized (New design, Cu metal plane changed to metal strips)			6% (better)

Figure 12: Proposed planarized substrate with metal strip design

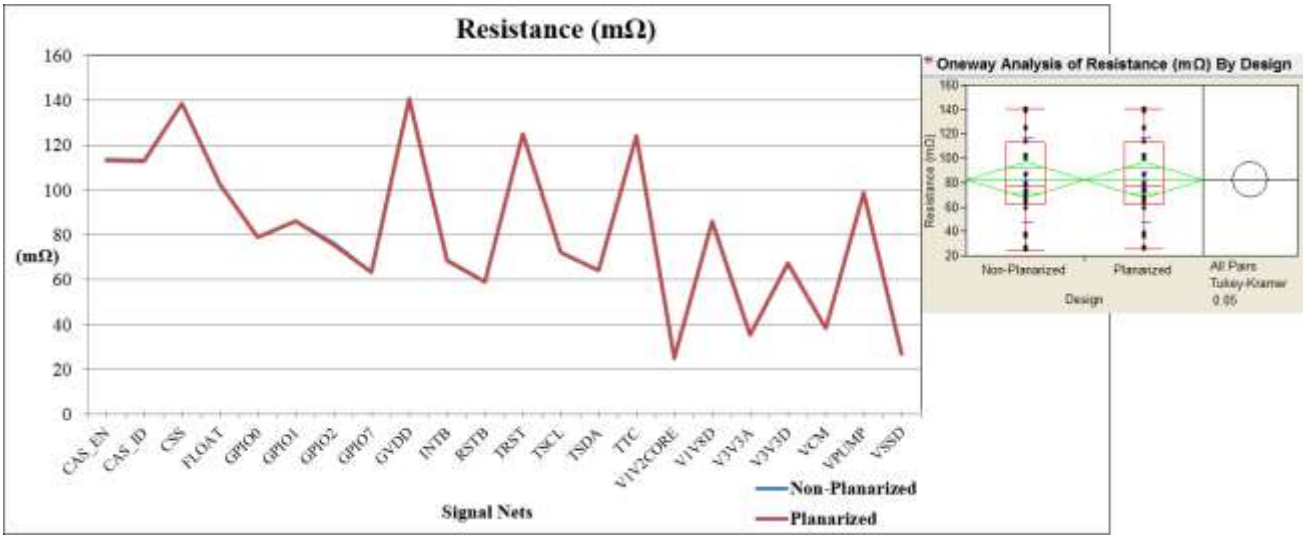


Figure 13: Resistance comparison of signal nets between 2 designs

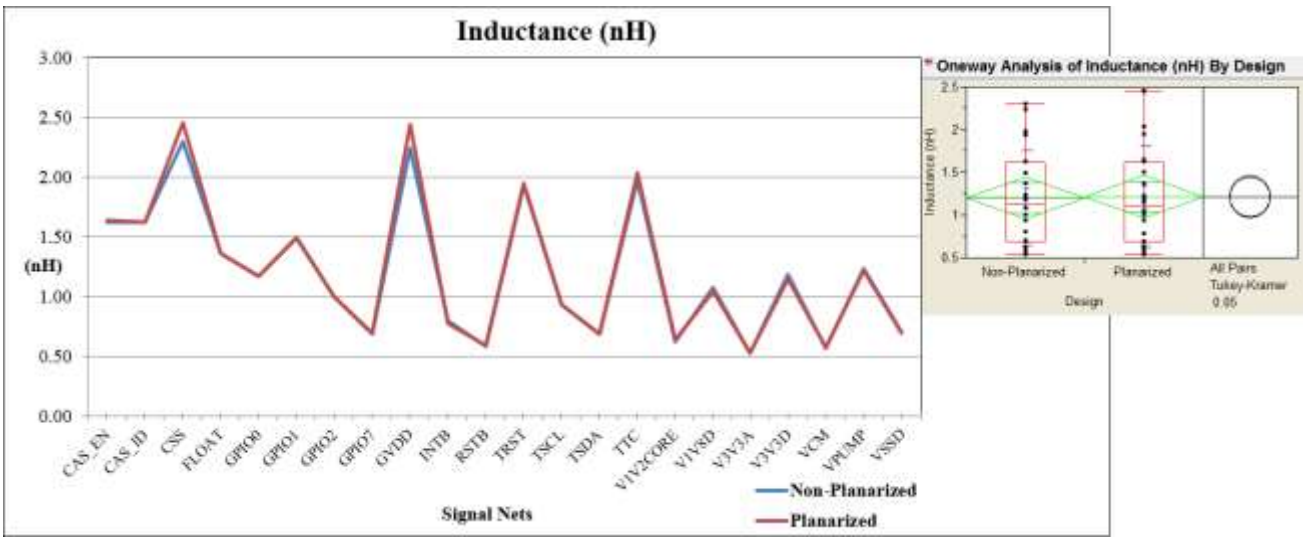


Figure 14: Inductance comparison of signal nets between 2 designs

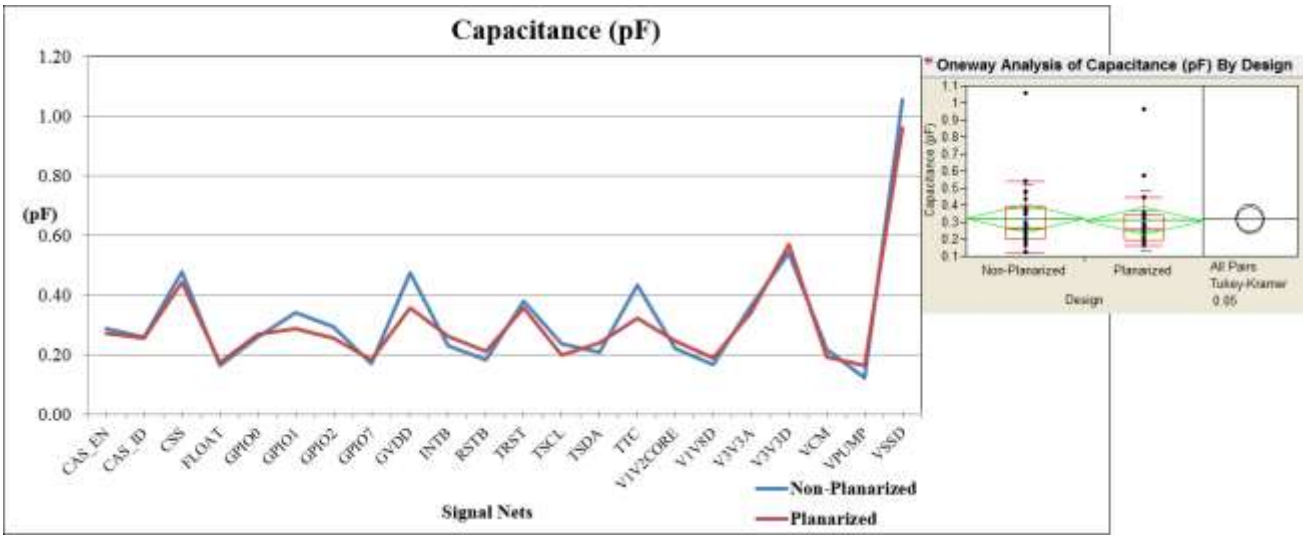


Figure 15: Capacitance comparison of signal nets between 2 designs

Based on the results, it is highly recommended to optimize DAF selection and substrate design when developing stacked die. Since this study focused on substrate design to eliminate delamination and voids, it is also recommended that DAF selection should be considered to ensure robustness of material selection.

6. ACKNOWLEDGMENT

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