Design and Simulation of a New Front-end Read-out Circuit based on Switched Capacitor Array (SCA)

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ABSTRACT--- ***In this paper, a switched capacitor array (SCA) for front-end read-out circuit of silicon strip, Si(Li), CdZnTe and CsI detectors, etc., which has 7 channels and 448 sample/hold cells with up to 2 MHz sample rates, is designed. The circuit is completely made by CMOS technology and 64 switched capacitors per channel are used to record 7 parallel analog transient signals. Trigger and clock are provided by the combination of several counter rings with a number of logic chips. The readout is made in column and permits to read the entire channel at more than 32MHz rate. This paper will also describe a novel T-Network configuration which is used to eliminate leakage current in the reset switch for each integrator, and a Clock generator which is used to optimize the gate logic to ensure nonlinearity of the SCA less than 0.2% at the 2MHz sample rate.***

Keywords--- Switched capacitor array, Sample and hold, Transient recorder, Transient digitizer, leakage current

1-INTRODUCTION

Switched Capacitor Arrays (SCAs) are compact, efficient and inexpensive analog signal recorders. They are used to acquire brief analog transient waveforms or take periodic measurements of analog signals [1, 2]. They are exceedingly low cost, low power, high density and easy to use as a replacement for ADC and digital memory combinations. A several hundred thousand individual waveform recording channels with massively parallel data acquisition systems are required in the experiments of nuclear science and astrophysics. The general task is the extraction and temporary storage, followed by slower readout, of brief but high speed analog transients. For many applications, acquisitions with higher sampling rate are needed [3]. Usually, a trigger decision is made to judge the value of the stored signals. Those signals are then discarded or digitized, processed, and transferred to computer system. Thus, these systems usually require both time delay via temporary storage and time stretching of the stored signal to match the performance of the data processing system.

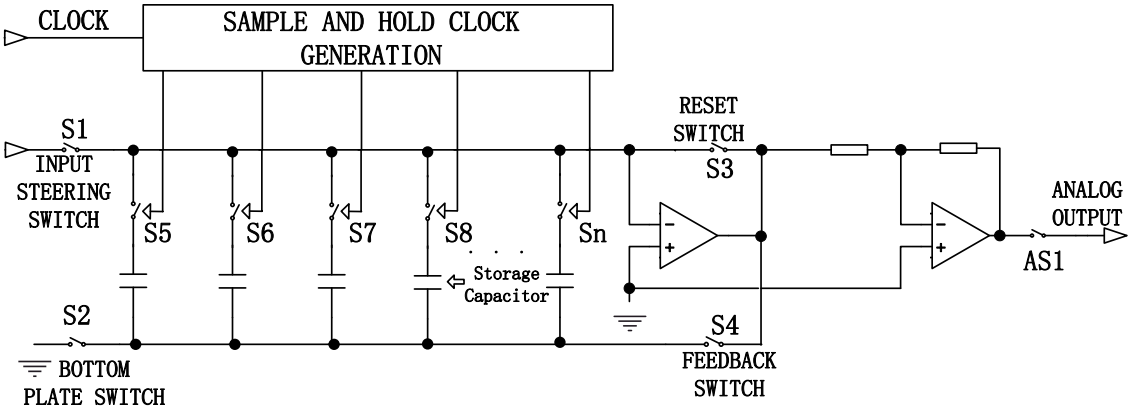

Fig. 1: Simplified circuit of a single channel.

Traditional solutions to this problem have involved the use of flash analog to digital converters (FADC's) followed by digital memory, or use of charge coupled device (CCD) delay lines. The switched capacitor approach may offer lower cost, lower power and higher density, and meanwhile providing fast sampling speeds, wider dynamic range and a high degree of flexibility. These performances are suitable for enhancing signal processing capability which may ultimately include pre-amplification, signal shaping, analog to digital conversion and sophisticated addressing schemes including sparse or selective data readout [2]. In this paper, a full switched capacitor transient analog waveform storage and waveform reconstruction of sample/hold cells has been designed and simulated. The SCA is organized with 7 channels of 64 serially addressed samples per channels with integrator, invert and multiplexed analog output. Signal sampling

frequencies is up to 2MHz. When many channels are involved, the timing diagrams should be carefully studied, developed and structured for proper actions.

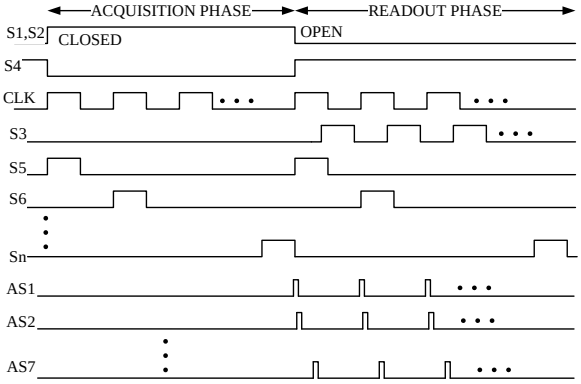

Fig. 2: Timing diagrams of 7channels.

2. CIRCUIT DESCRIPTION AND OPERATION

There are 1 decoder, 7 parallel analog signal inputs, 7 parallel analog outputs, 1 multiplexer and buffered analog output in the SCA. One digital clock input, four steering switch (S1, S2, S3, S4), and a digital subdivision clock output (synchronized on the main clock) are used to operate the circuit. Figure 1 shows simplified circuit diagram of a single channel, and Figure 2 is timing information of 7 channels.

The circuit contains 448 samples/hold cells subdivided into 7 parallel channels, 64 cells per channel. Each of the 7 channels has a dedicated analog input which steered a bus distributing the signal to 64 sample/hold cells. The input signal is transmitted through a complementary switch (S1). Each sample/hold cell consists of a complementary CMOS transmission gate and a 250 pF capacitor made by CMOS technology [4]. When complementary, rail to rail, clocks are applied to the gates of both transistors, transmission of analog signals from rail to rail can be accomplished. An externally supplied reference voltage is applied to the bottom plate of all capacitors through another switch (S2). The voltage stored on each sample/hold capacitor then corresponds to the difference between the input signals from a given channel at the time its sample/hold switch is opened and applied reference voltage. However the effect of leakage current in the (S3), reset switch will cause errors to the output of each channel in the long duration of these states. To eliminate this effect, the single reset switch (S3) was replaced by the T-Network configuration shown in Figure 3.

2.1 T-Network to prevent leakage current

While the sample/hold cell is in charge state, the reset switch has to be kept OFF. The effect of leakage current in the (S3), reset switch will cause errors to the output in the long duration of these states.

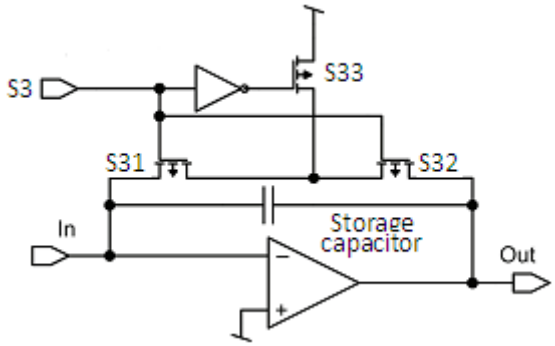

Fig.3 A T-Network configuration as the reset switch.

The leakage current of the CMOS switch is composed of the source to body reverse leakage current and the drain to source sub-threshold current. Since the source to body reverse leakage current can be negligible in CMOS, the drain to source sub-threshold current becomes the main factor of the "OFF" current.

The sub-threshold drain to source current I_{DS} of a CMOS transistor is an exponential function of the gate to source voltage V_{GS} and the drain to source voltage V_{DS}, and is given by

$$I_{DS} \approx K I_{D0} exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)\left(1 - exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (1)$$

$$I_{D0} = \mu C_{OX}(n-1)V_T^2 \quad (2)$$

where, I_{DS} is the drain to source current of the transistor, I_{DO} is the saturation current, V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, K is the aspect ratio $(=W/L)$ of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, $V_T(=k_BT/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the temperature, q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and n is the sub-threshold slope factor [5], [6]. Eq.(1) shows, even for $V_{GS}=0$, the only way to establish a zero switch leakage current is to set V_{DS} to 0 V. To maintain the V_{DS} of the CMOS switch at virtual ground, a T-Network configuration shown in Fig. 3 is used to replace the single reset switch (S3). The T-Network configuration is composed of two CMOS switches, (S31), (S32), in series and a grounded CMOS switch, (S33), attached to the node between the two switches. When the two CMOS switches in parallel with the storage capacitor are OFF, the third switch, (S33), is ON. Thus, in this configuration, V_{DS} of the switch connected to the inverting input of the integrator is maintained at 0 V, and zero or very little leakage current flows through this switch.

2.2 Clock generator

A counter ring based clocking mechanism sequentially turns ON and OFF sample/hold switches using a controllable break before making action. Break before makes insure that no charge sharing between subsequently engaged capacitors can occur. Break before can be controlled by varying the amount of time between non-overlapping clock phases. The 64 clock signals for sample/hold are generated once and shared by all channels for lower consumption and higher density. The sample/hold clock generator is designed to capture one sample per clock phase, so one sample captured per clock cycle reduces external clock generator.

Before readout, the analog input and reference potential steering switches (S1 and S2) are turn OFF, disconnecting the signal bus and bottom capacitor plate from the input side of the circuit. The reconstruction operational amplifier, in each channel, can then be connected to the sample/hold arrays via (S4). The readout sequence then proceeds in much the same way as the acquisition phase; under control of the ring counters, each sample capacitor is placed, sequentially, in the feedback path of the reconstruction Op-amp. Once the amplifier outputs have settled, multiplexing of all 7 channel amplifier outputs through a single buffered analog output can be accomplished. This allows all data from entire SCA unit to efficiently share a single high resolution analog to digital converter. After reconstruction and readout of each sample, stray charge on the sample capacitors and signal distribution busses are cleared by shorting each amplifier inverting input nodes and output nodes via (S3) switch. This prevents charge remaining on parasitic nodes from the previous samples to influence the next sample read out. Reset of the sample capacitors also prevents influencing next acquisition from any memory effect. To operate this, 3 JOHNSON Ring Counters (*DC4022B*) are used in series with several AND logic gates and complementary switches. The first Counter ring generated 8 pulses which are connected on 8 blocks (one block is made of 8 logic AND gates). The second counter ring enables each of those 8 blocks progressively to produce the 64 addressing signals, shown in Fig.4. And the third counter ring sends switching signal to ON/OFF (S1) and (S2) at the input of each channel, and the feedback switch (S4) at the reconstruction operation amplifier.

To perform the real time access, readout sample and reconstruction, the simulation was carried on *Proteus software* [7] for choosing components such as many Counter JOHNSON *DC4022B*, several logic AND gates and many complementary switches, realizing decoder and fast time access. Also at the same time this control system is synchronized with the output of different channel via a divider *74393*, a dual 4-stage binary counter. The synchronization starts after transient capture of the all channels; the readout is operated in column. It reads the first column of each channel, then one after another till the last columns. Therefore the entire reconstruction looks like simultaneous readout up to 32 MHz sample rate relative to 2MHz sample rate during transient capturing, shown in Fig. 5.

3. CIRCUIT PERFORMANCE

Table 1 Performance summary.

Parameters	Values
Number of channels per chip	7
Number of storage cells per channel	64
Total storage cells per chip	448
Non-linearity within ± 2 Volts range	0.2%
Sample and hold time constant	12.5 ns
DC Gain at 2 MHz sample frequency	-0.63
Capacitor of array	250 pF
Input Voltage range	< 5 V
Output Voltage range	< 5 V
Acquisition rate	2 MHz
Readout rate maximum	32 MHz
Dynamic input range	10 to 2000 mV

The performance of the circuit is summarized in the table 1. With a 2MHz sample rate during acquisition phase, a 32MHz readout sample rate, and using ± 5 Volts supply. The proper operation to 2MHz sampling frequencies has been verified and the time constant for charging the sample/hold capacitors is 12.5ns. Storage droop rate due to leakage current flows through a single (S3) reset switch is about 60mV per ms. When the reset switch is replaced by a T-Network, this value goes down to 2mV per ms. Readout of all 448 samples using a multiplex output can be accomplished at 2MHz the same rate as acquisition rate.

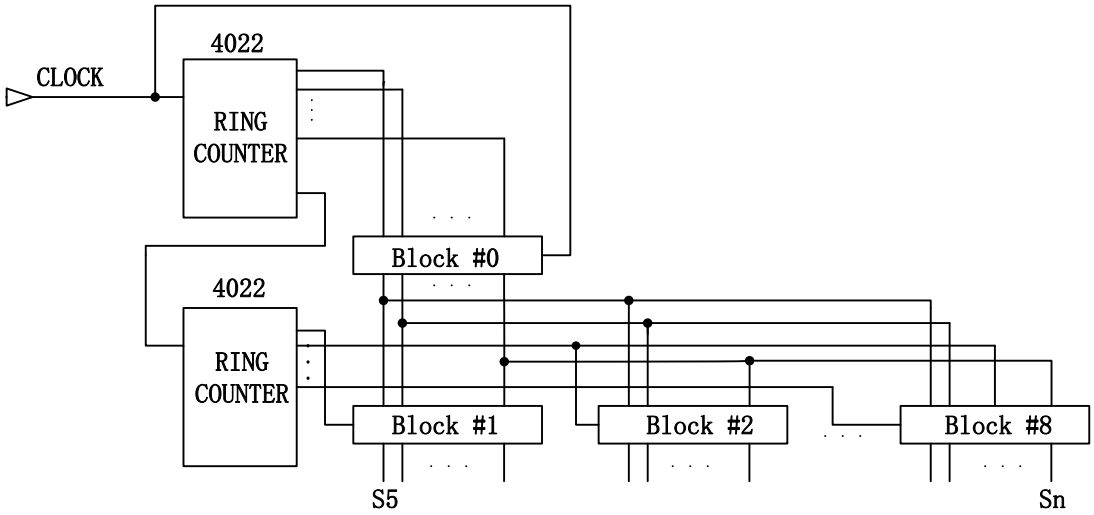

Fig. 4 Clock generator.

4. LIMITS ON CIRCUIT PERFORMANCE

The SCA circuit uses complementary switches 74HCT4066 exclusively in analog signal path. This maximizes the acceptable dynamic range of input voltage; it can store signals rail to rail. The readout operational amplifier in the SCA unit then becomes a limitation of the dynamic range. The linearity will be not good when output tends to the margin of the usable range from each rail.

The analog input signals shown in Fig.6 are fed to each channel respectively and the readout are shown in the Fig. 7. The time constant causes the gain of the system to drop uniformly because the system operates relativity at the high sample rates, also there serious nonlinearity after 8 rate samples running. This irregularity is due to the transition operated on the clock edge, each ring counter has 8 outputs. This can be further reduced by using a technique permitting a fast transition or using a fully differential technique. For exploitation of the circuit, the integral nonlinearity has been measured and the results are shown in Fig.9. The integral nonlinearity is closed to 0.2% from 10 mV to 2000 mV for analog input signals.

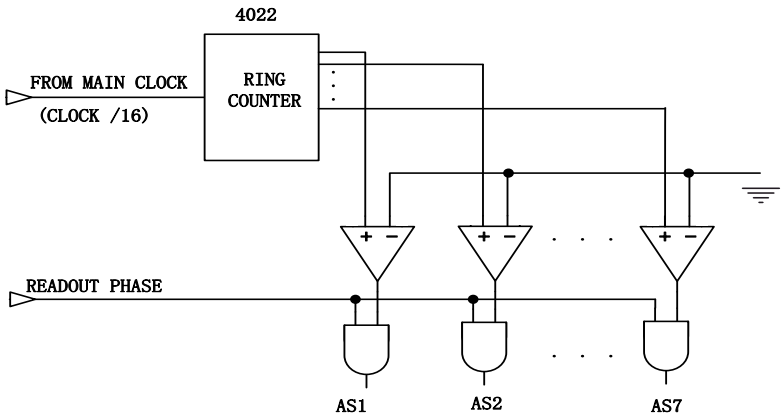

Fig. 5 Clock control readout sample

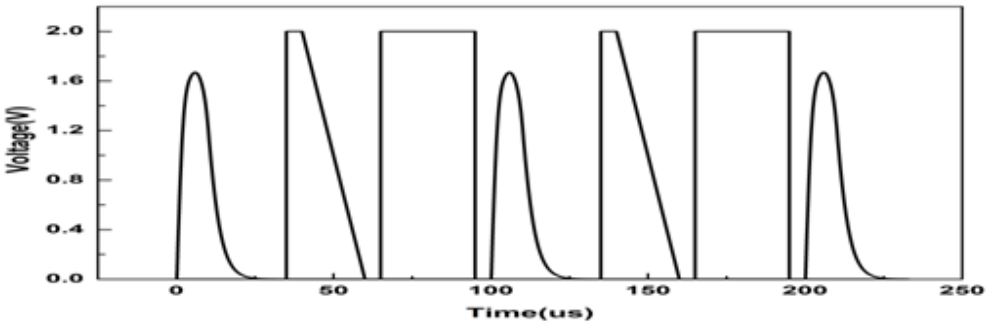

Fig. 6 Analog input signals.

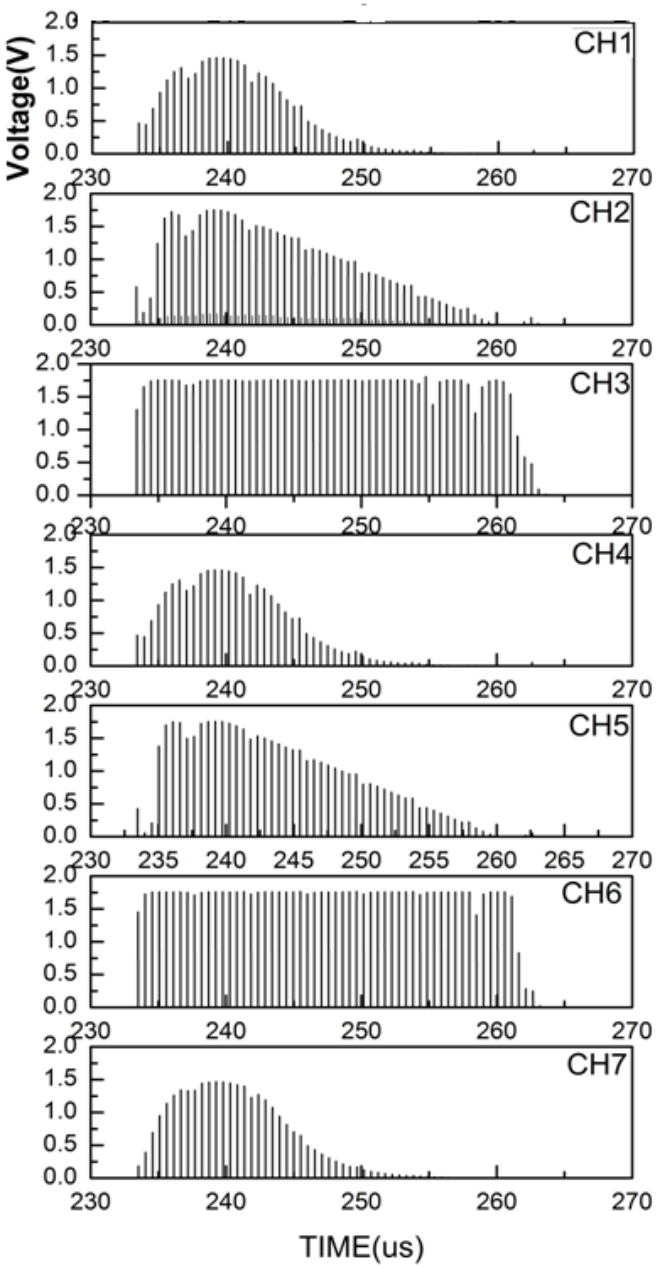

Fig. 7 Simultaneously analog output reconstruction for 7 channels

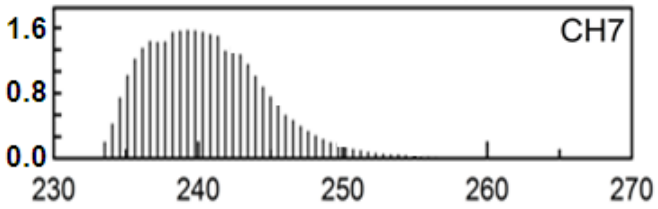

Fig.8 Reconstruction for channel 7 with T-Network replacing single reset switch (S3)

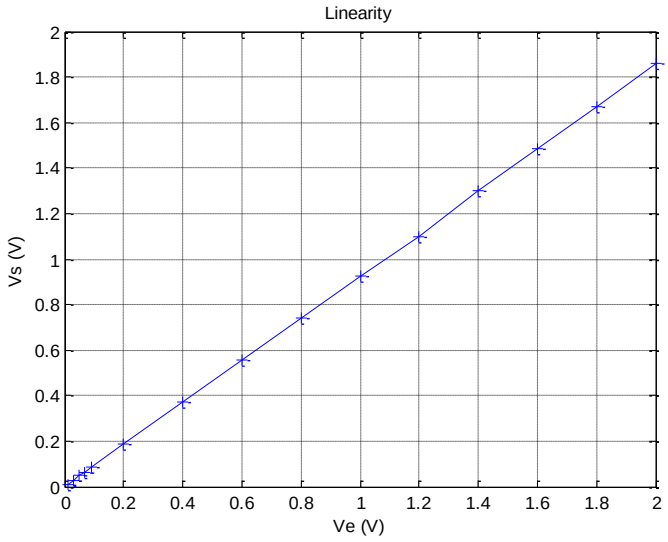

Fig. 9 Measured Nonlinearity for one channel.

5. FUTURE IMPLEMENTATIONS

To increase intrinsic dynamic range further, it may be necessary to use fully differential techniques. This would further reduce systematic errors, in principle, toward zero. Linearity can be improved by increasing the gain of readout amplifier and reducing parasitical capacitances. It is important to note that most analog performance parameters are sensitive to the number of samplers per channel that the circuit includes due to increased parasitic parameters associated with each sample cell.

6. CONCLUSIONS

The design and simulate a parallel data acquisition system has been made with capacitors and switches for each cell. We succeed to combine 7channels in the system, the input and output of the system are been controlled by a clock generator, a decoder and a multiplexer. The results shown in fig. 7, give - 0.63 for the Gain with the 2MHz sample frequency and with the T-Network to prevent leakage current, the results improve significantly in fig. 8. The chosen frequency limits the number of channels and it is the reason why we did not increase the number of channels and the number cell per channel. A Ring Counter with a fast slew rate in the future will allow increasing the frequency, therefore the number of channels. Our first step in this mini project is to see how control quickly the input and output of a small number of parallel data transient systems and reduced leakage current which causes errors to the output of each channel. In the nearest further we will see how, by substituting some main components, to increase the frequency, the number of channels and improve the SCA performances.

7. ACKNOWLEDGMENTS

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