Noise Optimization of Readout Front Ends in CMOS Technology with PS Circuit

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ABSTRACT--- ***In this paper, the study of the noise optimization of the charge sensitive preamplifier (CSP) for silicon strip, Si(Li), CdZnTe and CsI detectors is presented. The power limitation in such systems is available while a good noise performance and a fast signal processing time are required. This paper describes the CSP noise for CMOS technology with a chosen detector capacitance 3pF and transistor gate length ranging from 0.13 µm to 2µm. In this paper the designed CSP, followed by a fast pulse shaper (PS) stage, the equivalent noise charge (ENC) obtained is dominated by the thermal noise of an input MOS transistor. Noise behavior is evaluated with the input transistor works in a moderate inversion region. These analyses are made using a simplified EKV (Enz, Krummenacher, Vittoz) model and MATLAB simulations using BSIM3v3 models. We show several novel aspects of the noise optimization of the CSP regarding the optimum transistor width and the optimum of the drain current, and the sensitivity of the ENC between this width and the drain current.***

Keywords--- Charge sensitive preamplifier, Noise, Pulse shaper, Moderate inversion, EKV model

1. INTRODUCTION

Charge sensitive preamplifiers (CSPs) are the most commonly used amplifiers for signals delivered by light, radiation and particle detectors. Some examples of these detectors are photodiodes, X-ray detectors and detectors for nuclear and particle physics. The CSPs are mainly used in applied research (X-ray spectroscopy in medicine, biology) and in basic research (high energy physics, nuclear physics, astrophysics). When connected to a detector, the CSP gives an output voltage pulse with the maximum amplitude proportional to amount of the charge delivered by the detector. The precision in the measurement of the electric charge depends on the output noise level of the detector-amplifier system. This means the transducer (system) must be fast in order to accurately determine the time of interaction and with low noise in order to measure the energy deposited by the interacting photon. In spite of the fact that a CSP is inherently a less noisy amplifying configuration, great efforts have been made to reduce the noise level even further [1].

The relevant signal of a radiation detection device is in most cases the total free charged generated by the particle entering the device.The electronics attached to the device is supposed to measure this charge. In addition the device should be able to measure particles with a high rate. The current development of semiconductor sensors is focused on building fast highly segmented detectors, which have good efficiency together with good energy resolution. This requires the multichannel readout Application Specific Integrated Circuits (ASIC) with a very good noise performance and a short processing time. A typical signal processing for a single channel is shown in Fig. 1. A current signal generated in a pixel or strip of a semiconductor detector is integrated on the feedback capacitance C_{fed} of the CSP. At the output of the CSP a voltage step signal is formed with an amplitude proportional to the total charge deposited in the detector. This signal is fed to a shaper amplifier which provides the required pulse shaping and noise filtration to maximize the signal to noise ratio. Further processing can be done in the analogue or digital processing blocks depending on the application requirements.

The CMOS technology is very attractive for designing of multichannel CSP due to its high level of integration and high impedance of MOSFET devices [1, 5]. However the requirements of low power dissipation together with the properties of submicron technologies introduce new factors which must be taken into account during the noise optimization of the CSP. These aspects are discussed in detail in this paper. The paper is arranged as follows. The existing methodology for a low noise amplifier design is discussed at first, pointing to its limitation for submicron CMOS processes. Then the simplified EKV model is presented and applied to the CSP noise optimization. The used of the EKV model analytical calculations with MATLAB simulations using BSIM3v3 models is done for different aspects of the CMOS technology. The results of the CSP noise optimization for technologies are presented. The choice of the optimal transistor width and of the drain current transistors as input devices are also discussed.

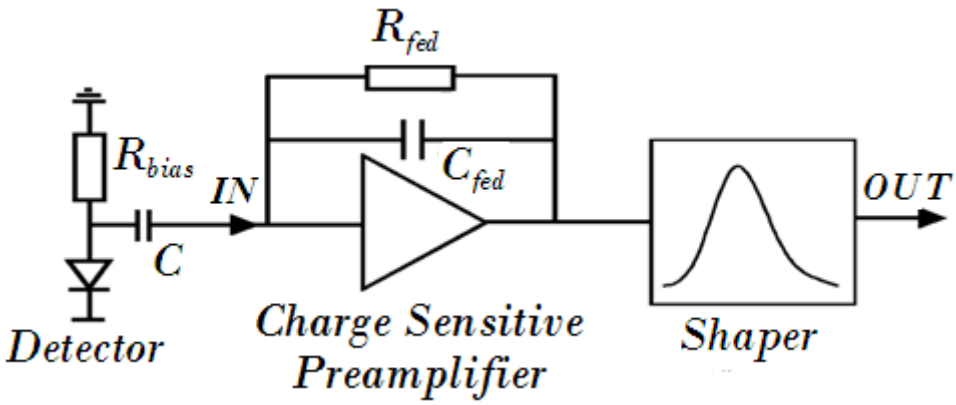


Figure 1: block diagram of detector readout system

2. CHARGE SENSITIVE AMPLIFIER AND NOISE SOURCES

The simplified noise model of a CSP is shown in Fig. 2. The noise performance of this system can be analyzed using the equivalent input voltage noise source and input current noise source.

In the well-designed CSP the voltage noise is dominated by the noise of the input transistor. In this transistor thermal noise occurs always, if the movement of a charge generates a voltage drop. This is the case in ohmic resistors as described, but also for instance in the conducting channel of a field effect transistor (FET). In this case the thermal noise generated in the channel corresponds to the variance of an equivalent noise voltage at the gate input.

$$V_{th}^2 = \frac{4KT\gamma n}{g_m} \quad (1)$$

where K is Boltzmann's constant, T is room temperature, $g_m = \delta I_{drain}/\delta V_{gate}$ denotes the forward transconductance of the FET, γ is gamma factor, n is the subthreshold slope factor.

In complex system often additional noise, with a *1/f* spectrum is observed, which is called flicker noise. It has different physical origins such as

$$V_{1/f}^2 = \frac{1}{C_{OX}^2 WL}\frac{K_f}{f} \quad (2)$$

The parallel noise current in figure 2 can come from various sources like the shot noise of the detector bias current, the thermal noise of bias resistor, a feedback resistor connected parallel to C_{fed} and a noise current source from the input FET of the amplifier. The shot noise evaluates numerically to:

$$i_{det}^2 = 2qI_0 \quad (3)$$

and the noise due to any resistor R_{bias} connected parallel to C_{fed} to:

$$i_{Bias}^2 = 4KT\frac{1}{R_{bias}} \quad (4)$$

Typical sensor bias resistors are of order 2MΩ per channel, the parallele noise from the bias resistor can thus be safely neglected. Typical feedback resistors R_{fed} needed to discharge C_{fed} are even larger.

Equivalent noise current density of the FET, in general, is the induced noise current density in the gate due to the capacitive coupling of the channel to the gate can be expressed as [6]

$$i_{GIC}^2 = \frac{32}{45}KT\gamma\frac{(2\pi fWLC_{OX})^2}{ng_m} \quad (5)$$

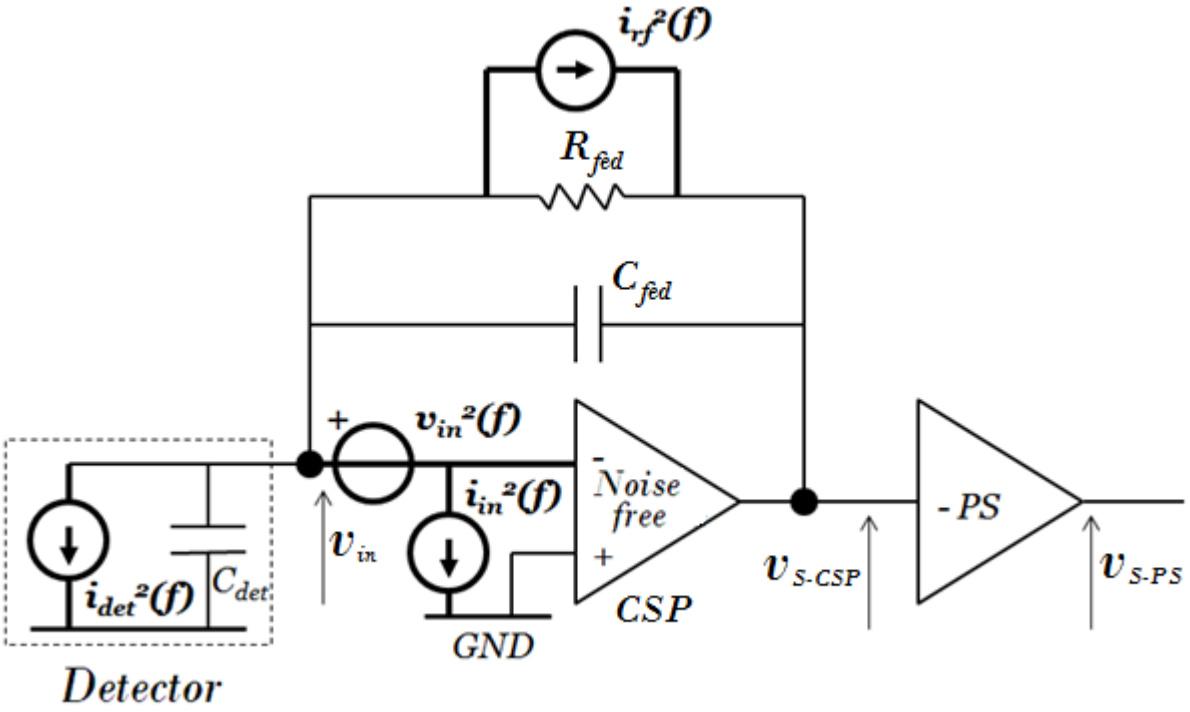


Figure 2. Noise model for a charge sensitive preamplifier coupled to a detector.

The noise generated by the input FET of the amplifier is represented by fluctuation of V_{in}. All subsecquent steps of the signal amplification generate of course also noise. However, due to the amplification the signal becomes larger and the noise to signal ratio smaller. Thus, in normal circumstances, the noise of the amplification chain with the exception of the input FET can be neglected as well. Now let's calculate the expected size of the noise due to V_{in} and I_{bias} as observed at the output of the amplifier:

Any voltage V_{in} will cause the differential amplifier to regulate its output by charging up C_f until an equilbrium is reached. The integrator amplifies the input current spectrum injected at V_{in} according to the equation:

$$H(s) = \frac{V_{s-CSP}}{I_d} = \frac{g_m}{\frac{g_m}{R_{fed}} + sg_m C_{fed} + s^2 C_{out}(C_{det}+C_{fed}+C_g)} = \frac{R_{fed}}{1 + sR_{fed}C_{fed} + \frac{s^2 R_{fed} C_{out}(C_{det}+C_{fed}+C_g)}{g_m}} \quad (6)$$

This equation describes in frequency domain, how the signal current and parallel noise is amplified in the integrator. We can see that overall equivalent noise voltage $V_{S\text{-}CSA}$ at the output of the amplifier equals

$$V_{S-CSP}^2 = V_{S-CSP-Th}^2 + V_{S-CSP-GIC}^2 + V_{S-1/f}^2 + V_{S-det}^2 \quad (7)$$

with

$$V_{S-CSP-Th}^2 = \frac{4KT\gamma n}{g_m}\left((C_{fed}+C_{det}+C_g)^2(2\pi f)^2 + \frac{1}{R_{fed}^2}\right)|H(s)|^2 \quad (8)$$

$$V_{S-CSP-GIC}^2 = \frac{32}{45} KT\gamma \frac{(WLC_{OX})^2}{g_m}(2\pi f)^2 |H(s)|^2 \quad (9)$$

$$V_{S-1/f}^2 = \frac{K_f}{f}\frac{1}{WLC_{OX}^2}\left((C_{fed}+C_{det}+C_g)^2(2\pi f)^2 + \frac{1}{R_{fed}^2}\right)|H(s)|^2 \quad (10)$$

$$V_{S-det}^2 = 2qI_0|H(s)|^2 \quad (11)$$

The chosen shaper (filter *RC-(CR)*^{3}) amplifies the $V_{S\text{-}CPA}$ further by *Vout(s) = G(s).*$V_{S\text{-}CSA}$*(s).* Although, *G(s)* is a complex function in general, variances obey the simple rule:

$$< V_{out}^2(\omega) >= |G(i\omega)|^2 \cdot < V_{S-CSP}^2 > \quad (12)$$

Adding these four contributions in quadrature and using (12) we end up with the variance of the total noise spectral density at the output V_{out} of the amplifier:

$$\frac{d\langle V_{out}^2\rangle}{df} = \left(\left(\frac{4KT\gamma n}{g_m} + \frac{K_f}{f}\frac{1}{WLC_{OX}^2}\right)\left((C_{fed}+C_{det}+C_g)^2(2\pi f)^2 + \frac{1}{R_{fed}^2}\right) + \frac{32}{45}KT\gamma\frac{(WLC_{OX})^2}{g_m}(2\pi f)^2 + 2qI_0\right)|H(s)|^2|G(i\omega)|^2 \quad (13)$$

To get the total noise at the output, this equation needs to be integrated over the full frequency range. It is conveniant to express the integrated noise fluctuation relative to the pulse height generated by a real signal of a given charge (calibration signal). The ratio between the square root of the variance of the noise fluctuations and the output calibration signal height per unit charge is called equivalent noise charge (ENC); it is usually given in units of electrons.

In order to find the ENC of a detector system one needs to calculate the noise *rms* value at the shaper output. Knowing the charge gain of the system the equivalent noise charge can be expressed as [7, 8]

$$ENC = \sqrt{\frac{\overline{V_{S-PS}^2}}{|V_{S-PS-Peak}|^2}}, \qquad V_{S-PS-Peak} = \frac{Q_{in}}{C_{fed}}\frac{A_S}{3!}\left(\frac{3}{e}\right)^3 \quad (14)$$

then

$$ENC_{th}^2 = \frac{e^6}{q^2}\frac{kT\gamma n}{g_m}\frac{1}{2592T_p}\left(3\left(C_{fed}+C_{det}+C_g\right)^2 + 5C_{fed}^2\right) \quad (15)$$

$$ENC_{gic}^2 = \frac{e^6}{q^2}\frac{kT\gamma}{ng_m}\frac{(WLC_{OX})^2}{4860T_p} \quad (16)$$

$$ENC_f^2 = \frac{1}{486}\frac{e^6}{q^2}\frac{K_f}{C_{OX}^2}\frac{1}{WL}\left(\left(C_{fed}+C_{det}+C_g\right)^2 + 3C_{fed}^2\right) \quad (17)$$

$$ENC_d^2 = \frac{5}{5184}\frac{e^6}{q}I_0T_p \quad (18)$$

$$ENC_{tot}^2 = ENC_{th}^2 + ENC_{gic}^2 + ENC_f^2 + ENC_d^2 \quad (19)$$

where C_g is the gate capacitance of the input transistor, C_{fed} the feedback capacitance and C_{det} the detector capacitance. T_p is the peaking time, i.e. the time at which the signal at the shaper output reaches the maximum.

The contribution of the shot noise of the detector decreases with the shortening peaking time, while the thermal noise and the induced noise current density in the gate contribution of the input transistor increase with the decreasing peaking time. The contribution of the input voltage flicker noise to the ENC is independent of the peaking time.

For MOS transistor in the saturation, g_m is the transistor transconductance and γ ranges from 1/2 to 2/3 depending on the channel inversion [9, 10]. The formula (19) could be modified by the excess noise factor connected with short channel effects like carrier heating, velocity saturation or mobility reduction. These effects are strongly technology dependent and can be effectively estimated only by systematic measurements. For this reason they are not taken into account in our analysis. However in the case of constant multiplicative excess noise factor, performed below analyses are still valid. Depending on a bias current of the CSP the input transistor can operate in a strong, moderate or weak inversion region.

3. DISCUSSION FOR NOISE OPTIMIZATION OF CSP

In readout front end systems the standard noise optimization in the strong inversion is not very useful since, as it was mentioned, the input transistor works usually in the moderate inversion region. For the moderate inversion region no simple formula describes the optimum noise behavior. In this case one of two approaches may be considered. The first one is to perform the MATLAB simulations for different drain current values and different transistor dimensions to find transistor transconductance and capacitance and use them to find the minimum ENC from formula (19). The second approach is to apply a simplified analytical EKV model [11, 13] in order to understand whether some general conclusions about the noise optimization of the CSP may be drawn. We have performed the analyses in both ways using the simplified EKV model for analytical calculations and using the results with MATLAB simulations performed with BSIM3v3 transistor model.

3.1 EKV model parameters

The EKV MOSFET model is a scalable and compact simulation model built on the fundamental physical properties of the MOS structure [9]. The EKV model was found to be quite successful in the moderate inversion region

[11, 13]. In particular, it was shown that the transistor transconductance calculated from EKV model agrees well with measurements. In its simplified version the basic parameters g_m, C_{gs}, C_{gb}, γ for MOSFET transistor working in saturation, may be calculated as shown below:

– Transconductance

$$g_m = \frac{I_D}{nU_T} f(i_f) \quad (20)$$

where

$$f(i_f) = \frac{1}{\sqrt{i_f + \frac{1}{2}\sqrt{i_f} + 1}}, \quad i_f = \frac{I_D}{I_S} \quad (21)$$

n is the subthreshold slope factor, $U_T = kT/q$ is the thermal voltage.

– Total gate capacitance is a sum of gate-source capacitance, gate-bulk capacitance and overlap capacitance

$$C_g = C_{gs} + C_{gb} + 2C_{ov}W \quad (22)$$

where C_{ov} is the overlap gate-diffusion capacitance per channel width while

$$C_{gs} = C_{ox}WL\left(\frac{3}{2} + \frac{1}{i_f f(i_f)}\right)^{-1} \quad (23)$$

$$C_{gb} = C_{ox}WL\frac{n-1}{n}\left(1 - \frac{i_f f(i_f)}{1 + \frac{3}{2} i_f f(i_f)}\right) \quad (24)$$

– Gamma factor

$$\gamma = \frac{1}{2} + \frac{1}{6}\frac{i_f}{i_f + 1} \quad (25)$$

As seen from the above equations apart from the model parameters one needs two additional technological parameters C_{ov} and n. While C_{ov} may be taken from the technology specifications, some assumptions should be made on the slope parameter n.

In moderate inversion region, the MOSFET has a two decade current transition from the weak to strong inversion. The right factor to determine the actual inversion level of a MOS transistor working in saturation is its normalized forward current *if* [10, 11]

$$i_f = \frac{I_D}{2n\mu C_{OX}(W/L)U_T^2} \quad (26)$$

Table1: Technology specifications *of CMOS* transistors

Symbole	***Définition***	***NMOS***	***PMOS***
K	Boltzmann constant (J/K)	$1.38.10^{-23}$	$1.38.10^{-23}$
T	absolute temperature (K)	298.15	298.15
q	Elementary charge (C)	$1.6.10^{-19}$	$1.6.10^{-19}$
Cox	gate oxide capacitance ($F.m^{-2}$)	$4.48.10^{-3}$	$4.48.10^{-3}$
K_f	flicker noise coefficient ($C^2.m^{-2}$)	$8.5.10^{-27}$	$8.5.10^{-27}$
K_p	transconductance Parameter ($\mu A.V^{-2}$)	181.10^{-6}	58.10^{-6}
n	Slope factor	1.22	1.17

3.2 Optimum input transistor width and gate length

We performed simulations for a set of input parameters covering the most frequently used range in the applications with the use of multichannel CSP, i.e. for

– Drain current between 0 up to 5mA,

– PMOS and NMOS transistor type (see table 1)

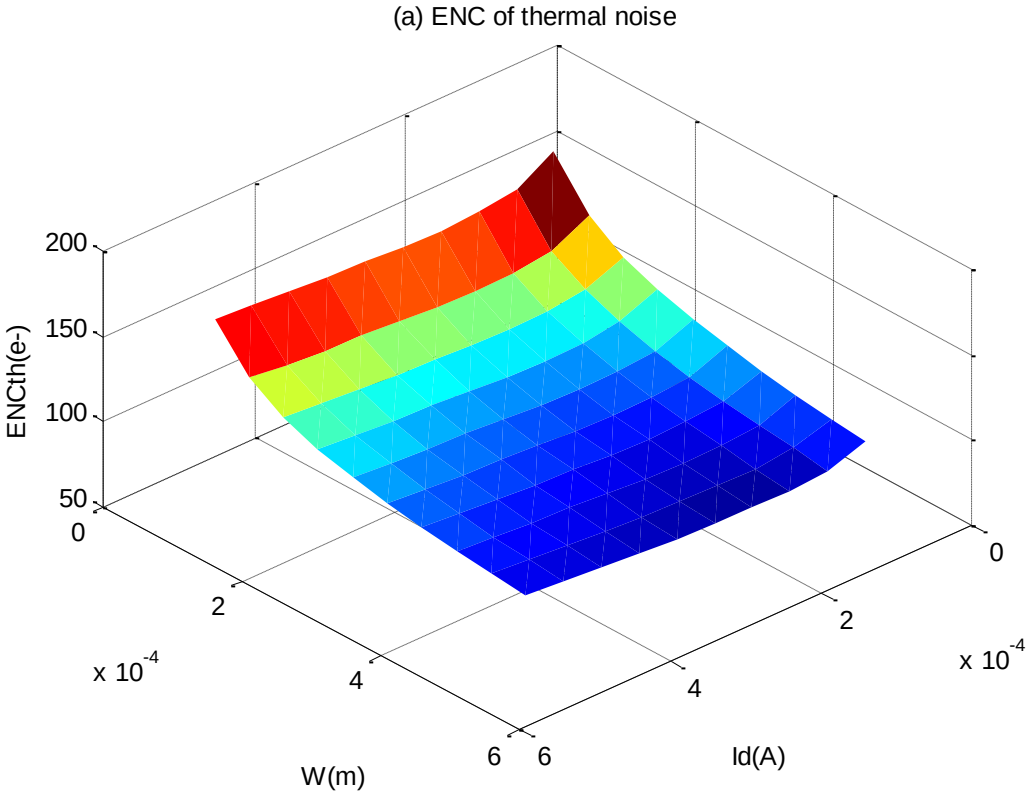
The simulations have been performed for a CMOS technologies size. Examples of the ENC plots vs. channel width and drain current of the MOS transistor for detector capacitance of 3pF are shown in Fig. 3. We have chosen gate length 2µm and the feedback capacitance C_{fed} = 100fF. To show the value of ENC we have assumed the shaper amplifier of $CR\text{-}(RC)^3$ type with the peaking time Tp = 50ns. From these Fig. 3 we conclude:

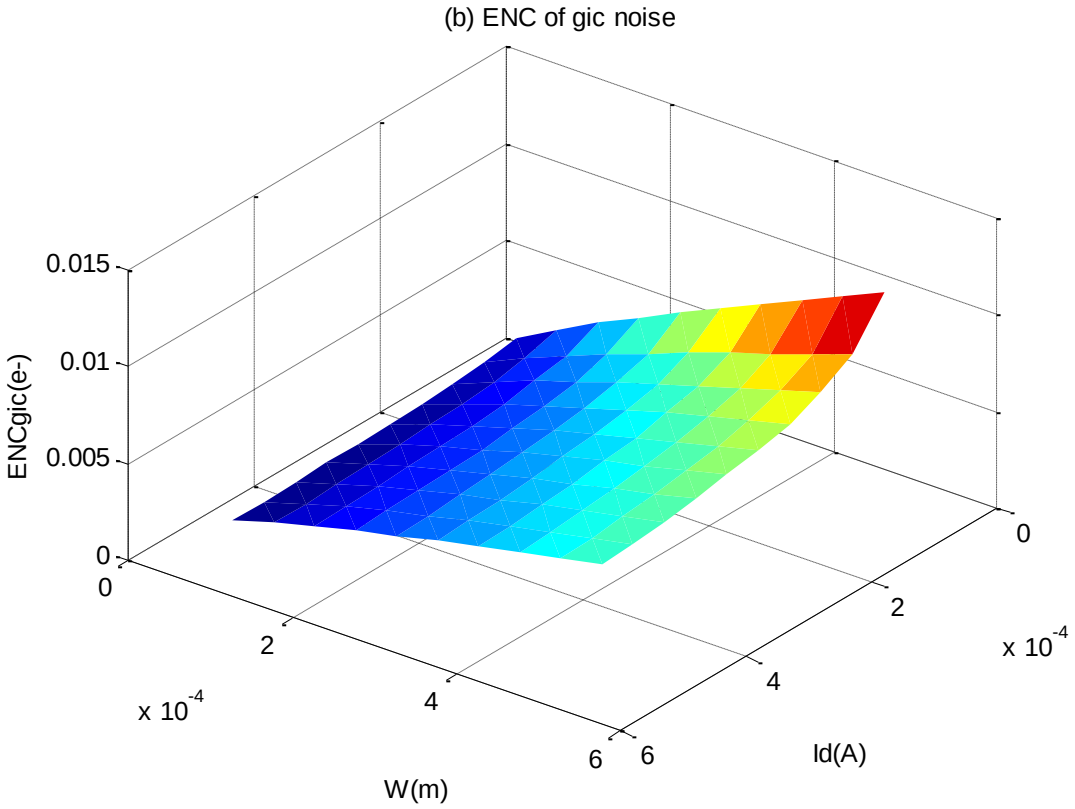
– The contribution of thermal noise decreases with the larger size technology and lower values of drain current, while the GIC noise contribution of the input transistor increases with the larger size technology and lower value of drain current. The contribution of the input voltage flicker noise to the ENC is slightly dependent of drain current but decreases with the larger size technology, while the shot noise of detector contribution is independent. For a fast signal processing considered in this paper (short peaking time Tp = 50ns) the ENC is dominated by the thermal noise of the input transistor.

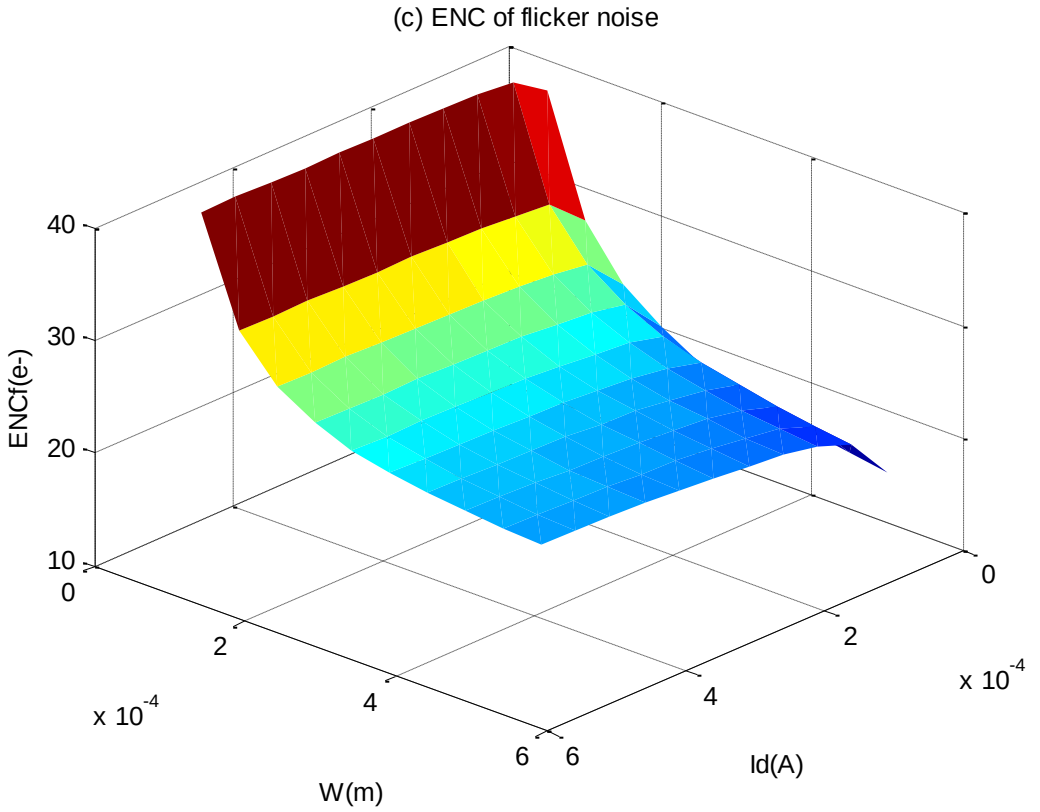
– The minimum ENC is more visible for larger size technology and lower input capacitance, while it flattens for larger size technologies; the flat region extends to very large values of the transistor width and drain current.

We have also performed the simulation for three different gate lengths: 2µm, 0.35µm, 0.13µm and the results are plotted in Fig. 3 (e), Fig. 4 and Fig. 5. One can see that:

– The minimum ENC is between the higher and lower gate lengths we have chosen; ENC is a nonlinear function of gate length.
– The wide range of choice of transistor width and drain current is very useful in the design of CSP since, the chosen width and drain current affects not only the total noise but some other important aspects like: the GBW of the amplifier.
– The wide flat ENC range around some values of the *W and* I_d gives the designer a large margin for the choice of the input transistor width and drain current.
– However for any gate length one can find a transistor width, which gives almost minimum ENC value for the whole current range.




(b) ENC of gic noise
ENCgic(e-)
0.015
0.01
0.005
0
0
2
4
6
x 10^-4
W(m)
0
2
4
6
x 10^-4
Id(A)


(c) ENC of flicker noise
ENCf(e-)
40
30
20
10
0
2
4
6
x 10^-4
W(m)
0
2
4
6
x 10^-4
Id(A)

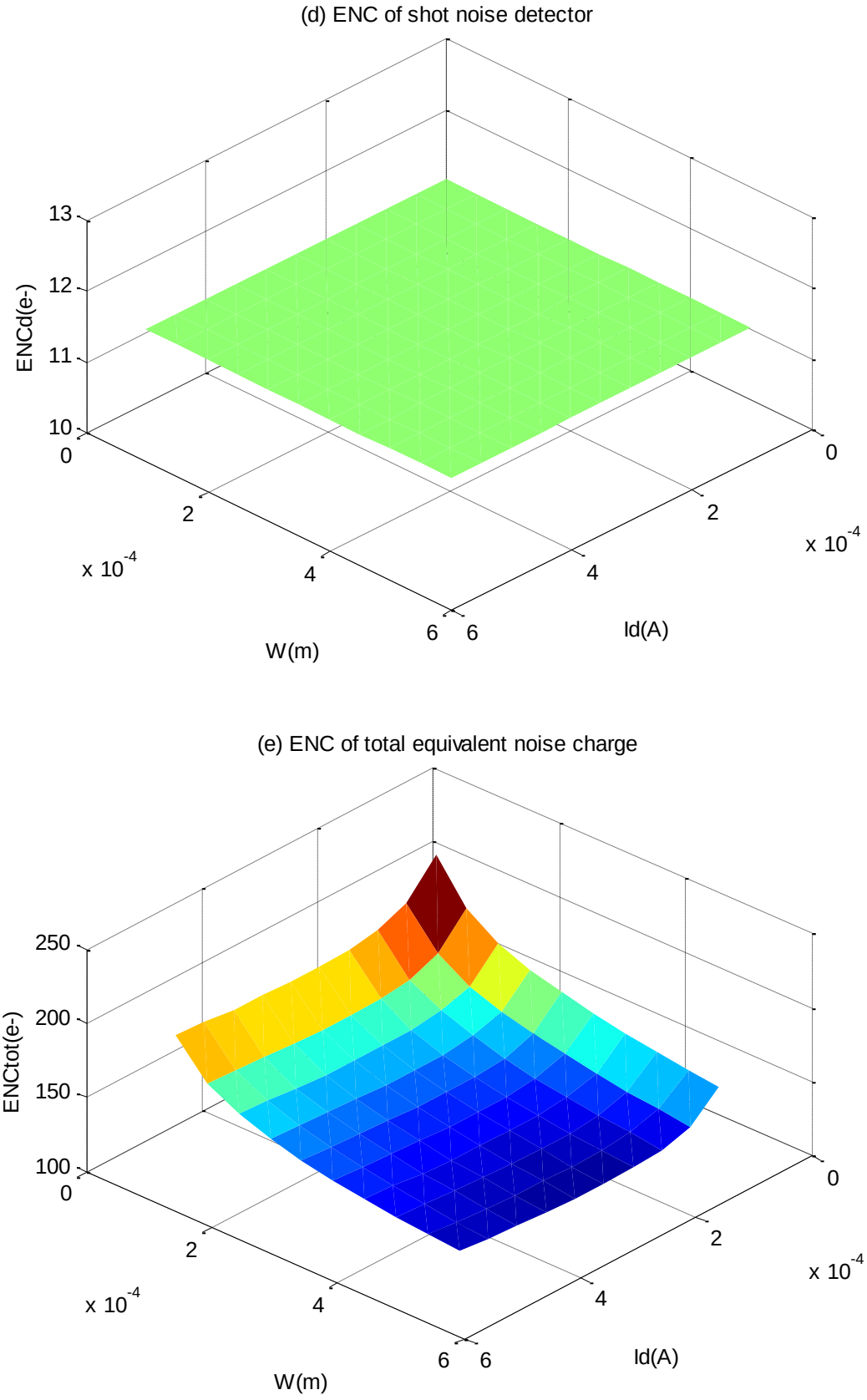


Figure 3 *ENC vs. MOS* transistor width (*W*) and drain current I_d: (a) *ENCth*, (b) *ENCgic*, (c) *ENCf*, (d) *ENCd*, (e) *ENCtot* for gate length (L) 2µm.

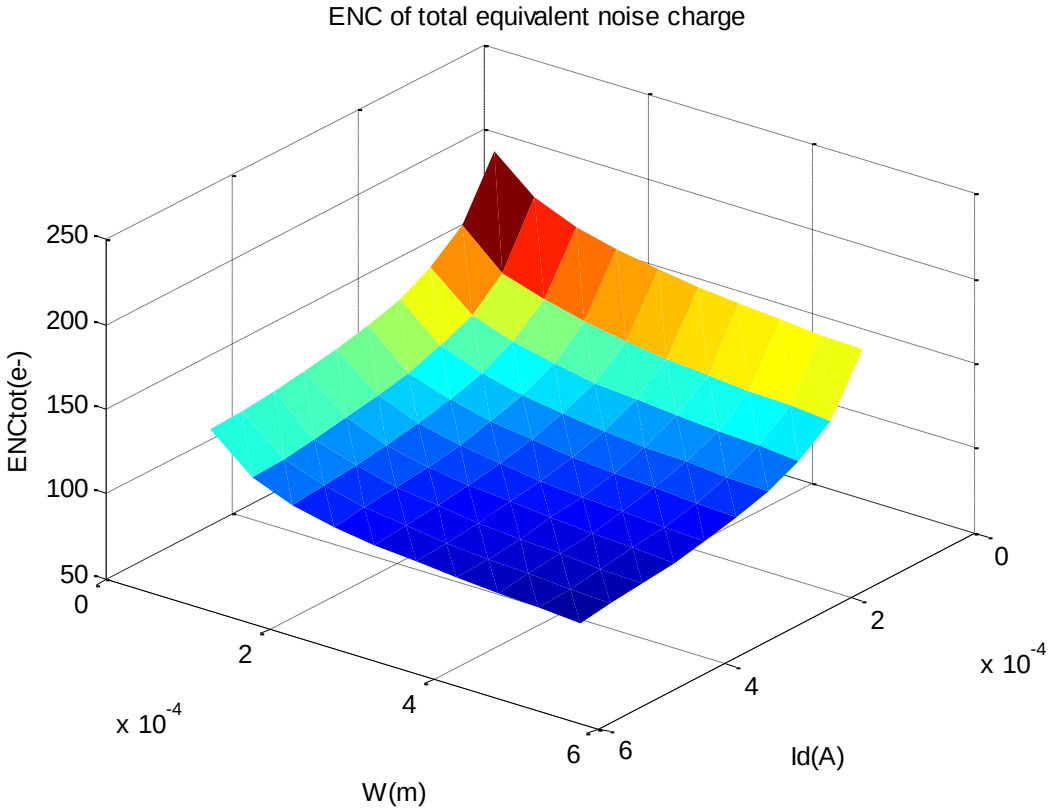


Figure 4 *ENC vs. MOS* transistor width (*W*) and drain current I_d; *ENCtot* for gate length (L) 0.35µm.

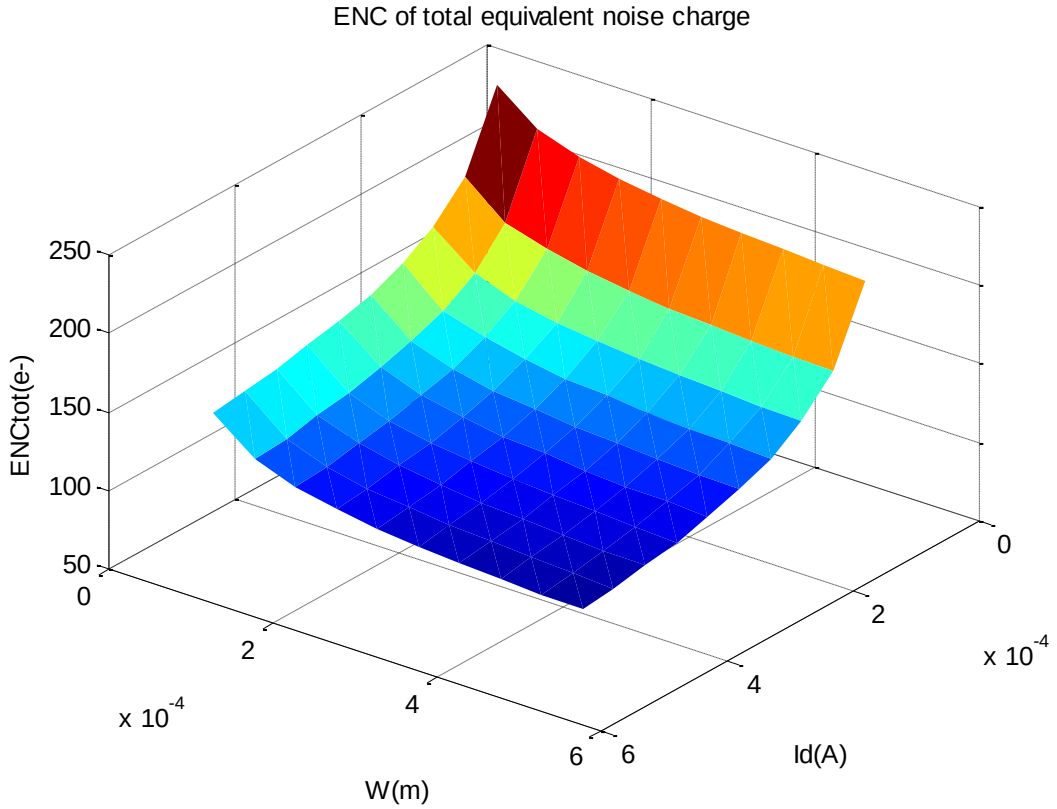


Figure 5 *ENC vs. MOS* transistor width (*W*) and drain current I_d; *ENCtot* for gate length (L) 0.13µm.

4. CONCLUSIONS

In the well-designed CSP, the power limitations with a good noise performance and a fast signal processing time are required. Since the input MOS transistor of CSP often works in moderate inversion. The noise estimation in this region requires proper noise modeling. A design strategy is described and simulated into MATLAB programming language. We implement analog block such as first transistor of Opamp into performance estimator. While calculating design parameters of the circuits, the analytical design equations of the EKV transistor model are used. From the performed simulations we confirm that the equivalent noise charge (ENC) is dominated by the thermal noise of an input MOS transistor and conclude that the designer has a wide choice of the input transistor width since the ENC dependence on width and drain current is very weak. Performance response graphs, which give ideas of circuit tradeoffs to the designers, were obtained. The future work will proceed in several directions. One of the directions is the incorporation of more subblocks and more circuits into the estimator.

5. ACKNOWLEDGMENTS

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